Faculty of Engineering &Technology (Co-Education) Department of Electronics and Communication Engineering	ECE Dept.	2024-25 (Even Sem)

Department of Electronics & Communication Engineering

ACTIVITY REPORT

Title of the Event	**Two day workshop for students on " VLSI FRONT-END DESIGN"**
Date of Activity held	08/06/2025 to 09/6/2025
Time of Activity	10:00 AM - 5:00 PM
Type of Activity (Cultural/ Cocurricular/Curricular)	Co-Curricular Activity
Chief Guest	**Mr. Sharan Koti**
Professional details of Chief Guest	FPGA Lead Engineer at Valeo, Hyderabad
Program/Course/ Class	Students workshop
Number of Staff attended	58
Activity Incharge	Dr. Rekha S and Dr. Mahesh R K
Description of Activity	On Day-1-8-6-2025 the Session started with Introduction to VLSI & Industry What is VLSI?, Application in chips, mobile, automotive, , VLSI job roles: Front-end, Back-end, Verification, DFT Skills required for front-end VLSI engineer, Front-End VLSI Design Flow, HDL Design (Verilog/VHDL basics), Functional simulation, Synthesis, Static Timing Analysis (STA, RTL vs Gate-level vs Netlist, ASIC vs FPGA design flow, Activity: Quick walkthrough of a Verilog "4-bit counter" RTL example. In the afternoon session, Verilog Coding & Simulation, Verilog structure (module, inputs, always block, testbench), Writing a simple Verilog modul, Writing a testbench, Functional Simulation using ModelSim or open-source tool like Icarus Verilog . Activity: Hands-on demo (live or pre-recorded) – simulate a Verilog module. Synthesis & Timing Basics, What is logic synthesis, How RTL is mapped to gates, On Day-2-In the morning session covered the Introduction to synthesis tools (Yosys/OpenSTA/Synopsys Design Compiler), Constraints & timing reports, Show synthesis result and gate-level netlist. FPGA Introduction & Demo , FPGA basics (LUTs, Flip-Flops, Block RAM, IO), Introduction to Xilinx/Intel FPGAs, Overview of Vivado design flow, Bitstream generation & flashing, Simulated FPGA design or tool GUI walkthrough. The afternoon session was on- Career Guidance , How to prepare for VLSI career, Online resources, internships, certifications, Resume & interview tips. Successfully completed RTL design and verification of FIFO, 32-bit ALU, and UART Transmitter & Receiver using Verilog, Implemented testbenches for functional verification on Cadence's NCLaunch. At last speaker conducted the mock interview session and given tips to how to face the interview.

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Day-1 Session-1 Photograps

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Day-1-Session-2-Photographs-Hands on Session

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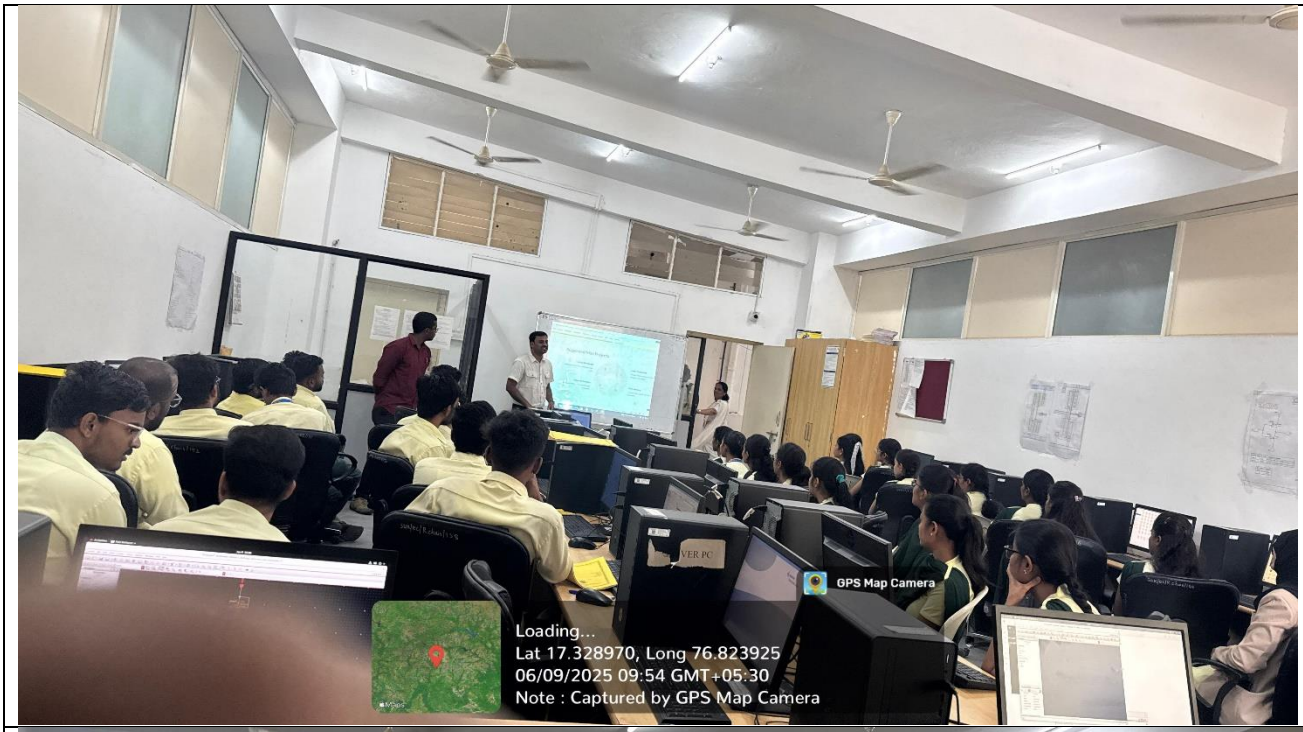

Day-2-Session-1 Photographs

Faculty of Engineering &Technology (Co-Education) Department of Electronics and Communication Engineering	ECE Dept.	2024-25 (Even Sem)

Day-2-Session-4- Photographs

Event Coordinator **Chairperson**