100+ Years of Glorious history inscribed in the yeomen service to the field of education

Centenary Celebrated Sharnbasveshwar Vidya Vardhak Sangha's

Estd. 2017
ಸ್ಥಾಪನೆ : 2017

ಶರಣಬಸವ ವಿಶ್ವವಿದ್ಯಾಲಯ
Sharnbasva University

Kalaburagi - 585103, Karnataka - India
ಕಲಬುರಗಿ ೫೮೫ ೧೦೩ ಕರ್ನಾಟಕ - ಭಾರತ

Phone / Fax No. 08472-277852, 277853, 277854, 277855 www.sharnbasvauniversity.edu.in - email : Sharnbasvauniversity@gmail.com

FACULTY OF ENGINEERING AND TECHNOLOGY (CO-EDUCATION)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Value Added Course

On

"Design Verification Using Cadence Tool"

About the Course: The value added course on **"Design Verification *Using Cadence Tool*"**, aim to introduce the most demand skills in VLSI. This course deals with the fundamental theory to Practical hand on training in Front End Design and Verification. This course allows the student to learn from the scratch to Design, write HDL code, Verification of the Design which help them to manage their projects efficiently and make the career as a VLSI Design and Verification engineer.

Highlight of the Course:

- 30 hours Course Duration
- Introduction to Digital Electronics, Verilog & System Verilog
- Practical training: How to Design using Verilog HDL.
- Practical training: Verification of the Design using System Verilog.
- Mini Project: Design to Synthesis of Counter
- Certificate (Min of 75% attendance)

Target Audience: UG/ PG

Course Experts:

Dr. Sharanagouda Nawaldgi

Advisory Committee:

Dr. Shashidhar Sonnad, Chairman, Dept. of E&CE, Faculty of Engg & Tech (Co-Ed), Sharnbasva University, Klb.

Dr. Shivakumar Jawaligi, Dean, Faculty of Engg & Tech (Co-Ed), Sharnbasva University, Klb.

Design Verification *Using Cadence Tool* Syllabus

[As per Choice Based Credit System (CBCS) Scheme]

SEMESTER-VI

Subject Code	18VL61	CIE Marks	NA
Number of Lecture Hour/Week	03+01	SEE Marks	NA
Total Number of Lecture Hours	30 Hours	Exam Hours	NA

CREDITS-04

Course Objectives: This course will enable students to:

- Understand the basic front end design flow.
- Understand the digital design concepts
- Understand the digital design using HDL.
- Learn the verification process in VLSI front end design.
- Learn the basic concepts of system verilog for verification.

Modules	**Teaching Hours**	**Revised Bloom's Taxonomy (RBT) Level**
Module -1		
Signals, Need of Digital signals, Introduction to digital electronics, Introduction to Boolean algebra, Positive and negative logic, switching circuits, Introduction to number systems, Data representation, Classification of codes, Logic gates, NAND gate as universal gate, NOR gate as universal gate, Combinational and sequential circuits, Examples, Clock.	**10 Hours**	**L1,L2,L3**
Module -2		
Introduction to Verilog HDL, Verilog data types, Modeling styles, RTL Example for Combinational and sequential, Introduction to IDE tools (Xilinx ISE, Cadence), Creating project example: Counter.	**10 Hours**	**L1,L2,L3**
Module -3		
Introduction to System Verilog, Data Types (Arrays, Strings, Unions, Structures), Interfaces, Interprocess Communications, OOPs, Dynamic Arrays, Associative Arrays and it's Usage, Randomization and Constraints , Functional Coverage, Assertions, DPI.	**10 Hours**	**L1,L2,L3**

Course Outcomes: At the end of the course, the students will be able to:

- Design a digital circuit for the given requirements
- Design digital logic using HDL.
- Develop verification environment for design verification
- Synthesize the digital design with the given constraints.

Text Books:

1.Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.

2. Chris SPeare, "System Verilog for Verification: A Guide to Learning the Testbench Language Features", Second Edition

STUDENT LIST

SL.NO	USN	NAME OF THE STUDENT
1	SG20ECE013	AISHWARYA S
2	SG20ECE019	ANKITA
3	SG20ECE023	B GUPTANK
4	SG20ECE024	BASAVARAJ
5	SG20ECE026	BHAVANA
6	SG20ECE027	BHIMASHANKAR
7	SG20ECE036	DRUSHTI BIRADAR
8	SG20ECE037	FARHAN AJMAL
9	SG20ECE038	FAROOQ PATEL
10	SG20ECE044	KAPISH V SHARMA
11	SG20ECE046	KEERTI
12	SG20ECE048	LAKANSINGH
13	SG20ECE049	MAHANANDA PATIL
14	SG20ECE303	SACHIN
15	SG21ECE500	AKSHATA
16	SG21ECE502	ARCHANALATA
17	SG21ECE503	AVINASH RATHOD
18	SG21ECE504	BHAGYSHREE
19	SG21ECE505	ILIYAZ ALI
20	SG21ECE510	SHAIKH AMEER PASHA
21	SG20ECE047	KSHEMALING
22	SG20ECE035	DRAKSHAYANI
23	SG20ECE045	KAVERI
24	SG20ECE053	MANANDA HANNUR
25	SG20ECE056	MEGHANA
26	SG20ECE060	NIDHI
27	SG20ECE069	PRAMOD SINGH
28	SG20ECE070	PRANAV A TURE
29	SG20ECE075	SANGEETA
30	SG20ECE077	SHASHIREKHA
31	SG20ECE079	SHIVANI R MALIPATIL
32	SG20ECE082	SHREELAXMI KULKARNI
33	SG20ECE083	SHRESTI CHARI
34	SG20ECE084	SHWETA
35	SG20ECE085	SONIKA
36	SG20ECE086	SOUMYA
37	SG20ECE088	SRUSHTI WALIKAR
38	SG20ECE090	SUKANYA
39	SG20ECE094	SYED ZABIULLAH HUSSAINI
40	SG20ECE096	VAISHNAVI
41	SG20ECE097	VAISHNAVI VINAYAK KULKARNI
42	SG20ECE098	VIDYA
43	SG20ECE100	ZOHA BUTOOL

Geo-Tag Photos