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Poojya Mahant Goddai Avaji



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A REPORT ON INTRODUCTION TO CIRCUIT AND LAYOUT DESIGN

(A three months value added course for Third-Year UG Program)

Academic year 2022-2023



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FACULTY OF ENGINEERING AND TECHNOLOGY [CO-EDUCATION]
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
VALUE ADDED COURSE
ON

"Introduction to Circuit and layout Design"

About the Course: The value added course on "Introduction to Circuit and layout Design", aim to introduce the most demand skills in VLSI. This course deals with the fundamental theory to Practical hand on training in VLSI. This course allows the student to learn from the scratch to write code, design using the CMOS transistors which help them to manage their projects efficiently and make the career as a VLSI design engineer.

High light of the Course:

- 30 hours Course Duration
- Introduction to Verilog & CMOS
- Practical training: How to write code using Verilog HDL Programming.
- Practical training: How to design Semicustom VLSI circuits using Cadence tools.
- Mini Project based on 45nm node
- Certificate

(Min of 75% attendance)

Target Audience: UG / PG

Course Experts: Dr. Anuradha Savadi, Associate Professor, Faculty of Engineering and Technology [co-education] , Sharnbasva University, Kalaburagi.

Alumni: Alumni Industry Engineers

Advisory Committee:

- Dr. Shivkumar Jawaligi, Professor & Dean, Faculty of Engineering and Technology [CO-EDUCATION] , Sharnbasva University, Kalaburagi.
- Dr. Shashidhar Sonnad, Professor & Chairman, Faculty of Engineering and Technology [CO-EDUCATION] , Sharnbasva University, Kalaburagi.

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INTRODUCTION TO CIRCUIT AND LAYOUT DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – VI

Subject Code	VALCLD-1	CIE Marks	0
Number Lecture Hour/Week	04	SEE Marks	0
Number of Lecture Hours	30	Exam Hours	0

CREDITS-00

Course Objectives: This course will enable students to:

- Learn to work in a Linux environment
- Understand the complete physical design flow
- Plan and execute implementations of systems
- Determine the performance of a system through simulation
- Establish capability for CAD tool development and enhancement

Modules	Teaching Hours
---------	----------------

Module -1

Basic electronics: BJT, MOSFET, diode, capacitor, resistor, inductor, current, voltage, ohm's law, KCL & KVL, conductor, insulator, semiconductor, STI (static time analysis) lab- schematic for NAND3, NOR3, AND4, OR4.	6 Hours
---	----------------

Module -2

CMOS Technology: Fabrication, CMOS inverter characteristics, lab-logic gate design, single stage amplifier (cadence 45nm tool)	6 Hours
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Module -3

Introduction to Digital layout: Standard cells, layout introduction, stick diagrams lab- standard cell design of basic gates.	6 Hours
--	----------------

Module -4

Introduction to Analog layout: process variations, layout dependent effects. Lab- any amplifier design.	6 Hours
--	----------------

Module -5

Physical design verification: LVS, DRC, DFM, HVDRC, Antenna effects	6 Hours
--	----------------

Course outcomes: After studying this course, students will be able to:

- Understand device physics and technology
- Hands on tool access
- Design any combinational and sequential circuits.
- Draw the layout for various schematics and run DRC, LVS

Text Book:

1. Behzad Razavi, —Design of Analog CMOS Integrated Circuits, TMH, 2007.
2. Alan Hastings- Art of Analog Layout, Edition. 2nd · Publisher. Pearson · Publication date. 21 July 2005

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Mahant of Sri Panchajanya
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Reference Books:

1. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.
2. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.

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BACKEND VALUE ADDED COURSE

DEPT OF ECE, FACULTY OF ENGG AND TECHNOLOGY [CO-EDUCATION]

SUBJECT: CIRCUIT AND LAYOUT DESIGN

SI NO	STUDENT NAME	USN
1	AKANSHA	SG20ECE015
2	AADIL KHAN	SG20ECE001
3	ABDUL RAHMAN	SG20ECE002
4	ABHISHEK ALLAGI	SG20ECE005
5	ANAND	SG21ECE501
6	ANAND MANAJI	SG20ECE017
7	ARCHANA	SG20ECE020
8	ARUN	SG20ECE021
9	BHARGAVI	SG20ECE025
10	BHOOMIKA DESAI	SG20ECE028
11	DEEPAK	SG20ECE032
12	GEETA	SG20ECE039
13	HARSHVARDHAN GAIKWAD	SG20ECE041
14	JYOTI	SG20ECE043
15	KARAN	SG21ECE506
16	MAHESH	SG20ECE050
17	MAHESH LADVANTHI	SG20ECE051
18	MALLIKARJUN	SG20ECE052
19	MANIKANTH	SG20ECE507
20	MD. MUBARAK	SG20ECE057
21	NAGARAJ	SG20ECE058
22	NIRANJAN	SG20ECE062
23	PRADEEP PATIL	SG20ECE066
24	PRADEEP	SG20ECE067
25	PRADEEP N D	SG20ECE068
26	PRASHANTH	SG20ECE509
27	RADHIKA	SG20ECE071
28	RAHUL SINGH	SG20ECE072
29	S SANNIDHI	SG20ECE073
-30	SAKSHI	SG20ECE074
31	SHAHEDA	SG20ECE064
32	SHARAN KUMAR	SG20ECE076
33	SHIVANI	SG20ECE078
34	SHRADDHA R P	SG20ECE081
35	SUDEEP EKLOOR	SG20ECE089
36	SUNIL KUMAR	SG20ECE091
37	SUPRIYA	SG20ECE092

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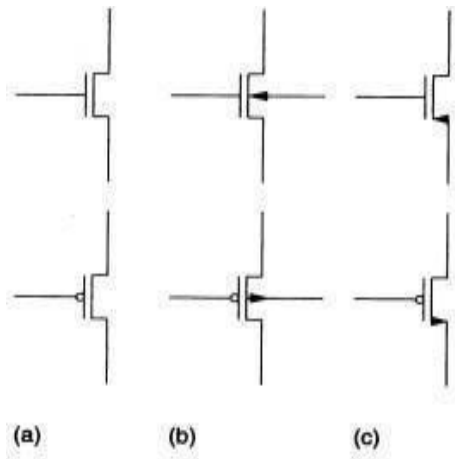
UNIT-1

MOS TRANSISTOR PRINCIPLE

INTRODUCTON

An MOS transistor is a majority-carrier device, in which the current in a conducting channel between the source and the drain is modulated by a voltage applied to the gate.

Symbols



NMOS

PMOS

NMOS (n-type MOS transistor)

- (1) Majority carrier = electrons
- (2) A positive voltage applied on the gate with respect to the substrate enhances the number of electrons in the channel and hence increases the conductivity of the channel.
- (3) If gate voltage is less than a threshold voltage V_t , the channel is cut-off (very low current between source & drain).

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PMOS (p-type MOS transistor)

- Majority carrier = holes
- Applied voltage is negative with respect to substrate.

Threshold voltage (V_t):

- The voltage at which an MOS device begins to conduct ("turn on")
- Relationship between V_{gs} (gate-to-source voltage) and the source-to-drain current (I_{ds}), given a fixed drain-to-source voltage (V_{ds}).

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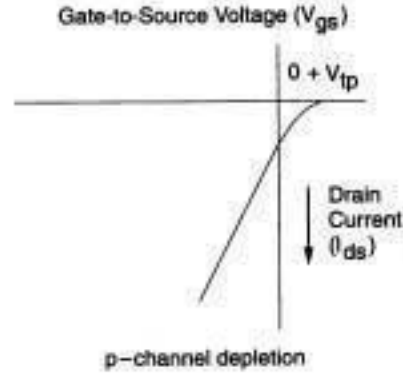
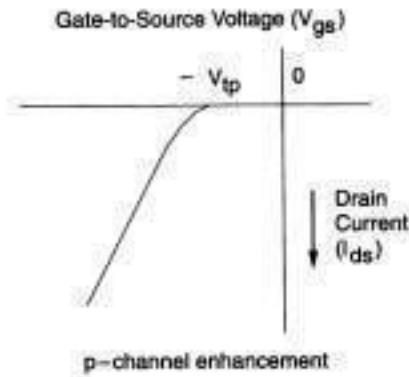
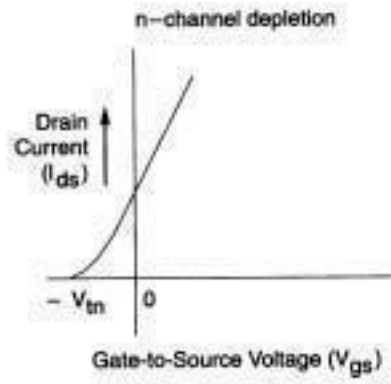
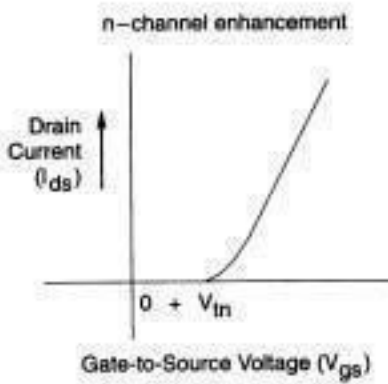


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- Devices that are normally cut-off with zero gate bias are classified as "enhancement-mode" devices.
- Devices that conduct with zero gate bias are called "depletion-mode devices"
- Enhancement-mode devices are more popular in practical use.

NMOS Enhancement Transistor

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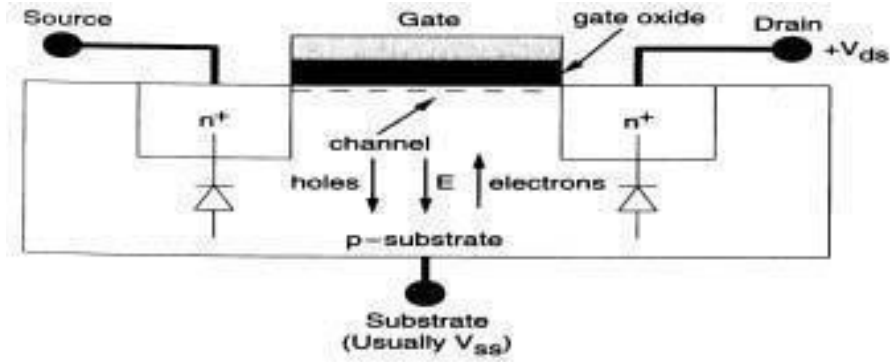


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It Consist of

- Moderately doped p-type silicon substrate
- Two heavily doped n^+ regions, the source and drain, are diffused
- Channel is covered by a thin insulating layer of silicon dioxide (SiO_2) called " Gate Oxide "
- Over the oxide is a polycrystalline silicon (polysilicon) electrode, referred to as the "Gate"

Features

- Since the oxide layer is an insulator, the DC current from the gate to channel is essentially zero.
- No physical distinction between the drain and source regions.
- Since SiO_2 has low loss and high dielectric strength, the application of high gate fields is feasible.
- In operation
 - Set $V_{ds} > 0$ in operation
 - $V_{gs} = 0$ no current flow between source and drain. They are insulated by two reversed-biased PN junctions
- When $V_g > 0$, the produced E field attracts electrons toward the gate and repels holes.
- If V_g is sufficiently large, the region under the gate changes from p-type to n-type(due to accumulation of attracted elections) and provides a conducting path between source and drain.
- The thin layer of p-type silicon is said to be "inverted".
- Three modes (see Fig 2.4)
 - Accumulation mode ($V_{gs} \ll V_t$)
 - Depletion mode ($V_{gs} = V_t$)
 - Inversion mode ($V_{gs} > V_t$)

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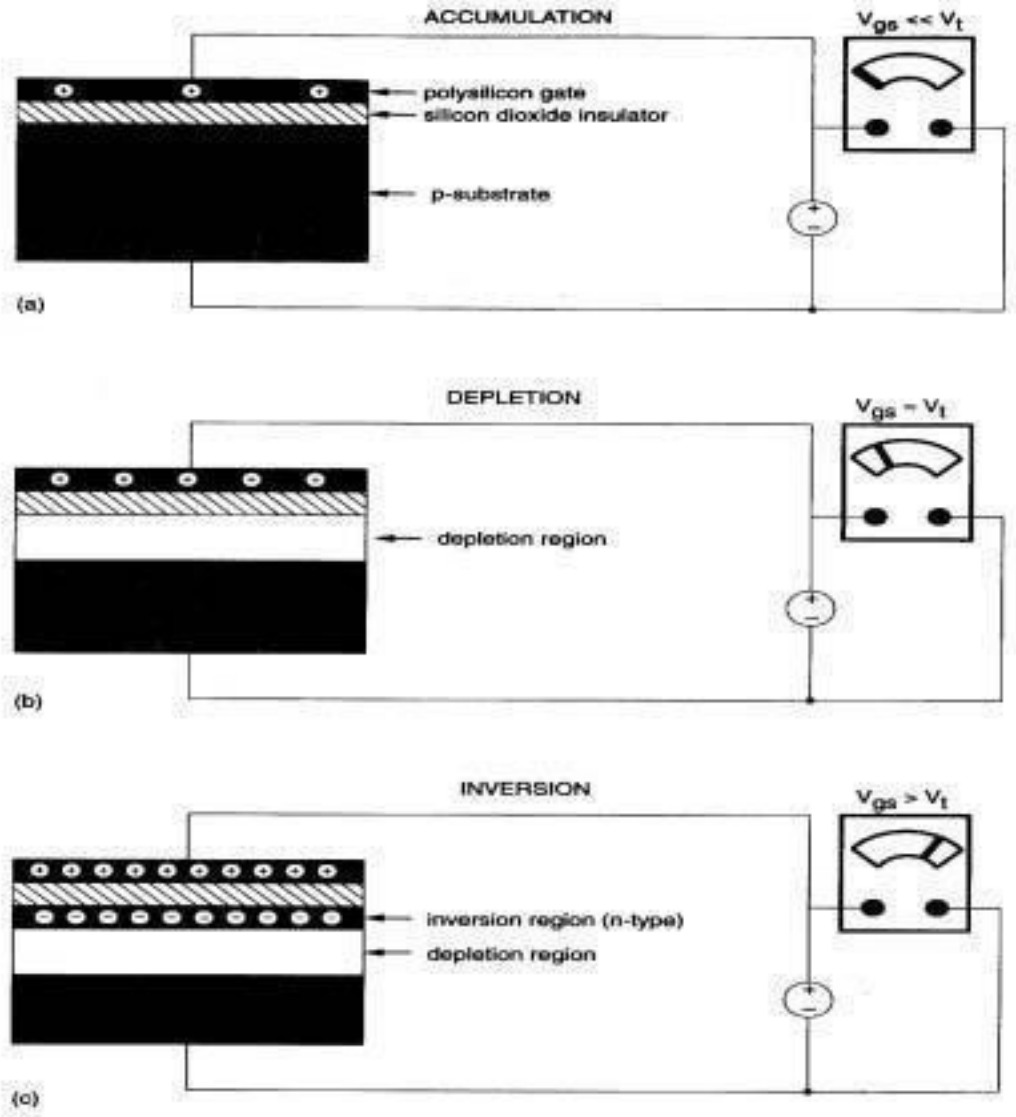


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Electrically

- (1) An MOS device can be considered as a voltage-controlled switch that conducts when $V_{gs} > V_t$ (given $V_{ds} > 0$)
- (2) An MOS device can be considered as a voltage-controlled resistor

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Effective gate voltage ($V_{gs}-V_t$)

At the source end , the full gate voltage is effective in the inverting the
channel.

At the drain end , only the difference between the gate and drain voltage
is effective

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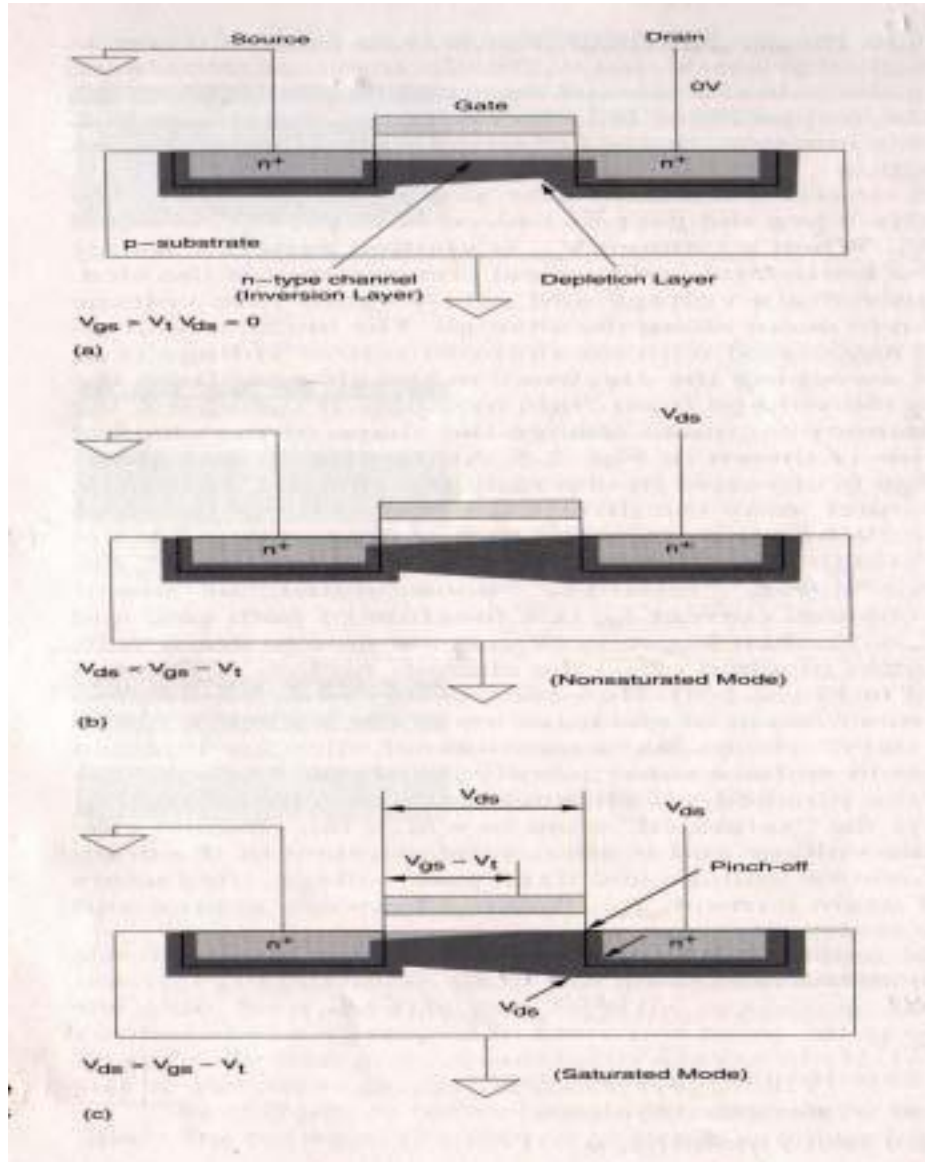


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Pinch-off

- $V_{ds} > V_{gs} - V_t \Rightarrow V_{gd} < V_t \Rightarrow V_d > V_g - V_t$ (V_g is not big enough)
- The channel no longer reaches the drain. (Fig 2.5 c)
- As electrons leave the drain depletion region and are subsequently accelerated toward the drain.

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- The voltage across the pinched-off region remains at $(V_{gs} - V_t)$
=> "saturated" state in which the channel current is controlled by V_g ,
and is independent of V_d

For fixed V_d s and V_g , I_{ds} is function of

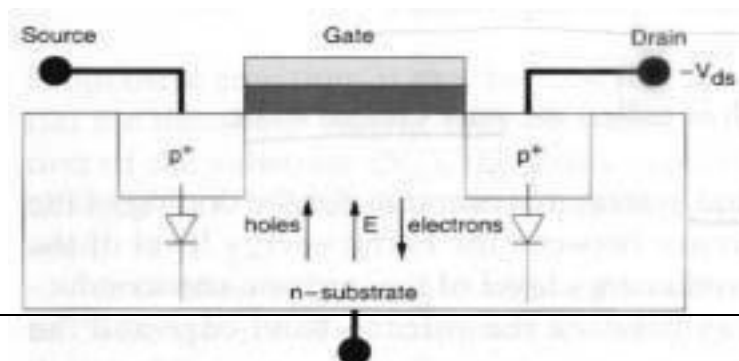
- Distance between drain & source
- Channel width
- V_t
- Thickness of gate oxide
- The dielectric constant of gate oxide
- (6) Carrier (hole or electron) mobility, .

Conducting mode

- "cut-off" region : $I_{ds} \approx 0$, $V_{gs} < V_t$
- "Nonsaturated" region : weak inversion region, when I_{ds} depends on V_g & V_d
- "Saturated" region: channel is strongly inverted and I_{ds} is ideally independent of V_d (pinch-off region)
- "Avalanche breakdown" (pinch-through) : very high V_d => gate has no control over I_{ds}

PMOS Enhancement Transistor

- $V_g < 0$
- Holes are major carrier
- $V_d < 0$, which sweeps holes from the source through the channel to the drain .



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Threshold voltage

- A function of
- Gate conductor material
- Gate insulator material
- Gate insulator thickness
- Impurity at the silicon-insulator interface
- Voltage between the source and the substrate V_{sb}
- Temperature
 - a. $-4 \text{ mV}/^\circ\text{C}$ – high substrate doping
 - b. $-2 \text{ mV}/^\circ\text{C}$ – low substrate doping

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SCALING

In scaling there are really two issues

- Devices Can we build smaller devices

What will their performance be try to avoid the wet noodle effect Wires

There is concern about our ability to scale both of these Components

Limitations

Limitations to device scaling has been around since working in 3m nMOS, 22 years ago (actually bipolar)

- Worries were
 - Short channel effect
 - Punchthrough
- drain control of current rather than gate
 - Hot electrons
 - Parasitic resistances
- Now worries are a little different
 - Oxide tunnel currents
 - Punchthrough
 - Parameter

control Parasitic
resistances

Transistor scaling

People are building very short channel devices

- Shown are I-V curves for 15nm L pMOS
- And a short channel nMOS
- The structure is strange
- FinFET
- But you can make them work

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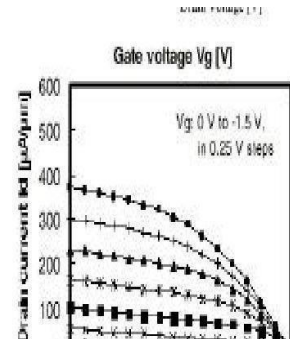
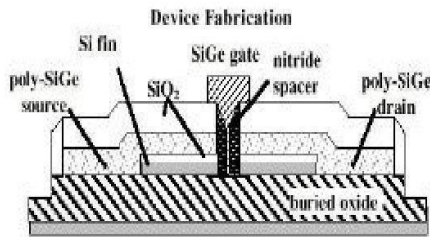
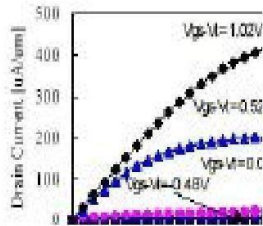


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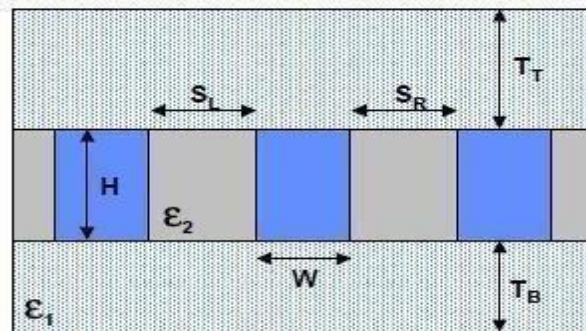
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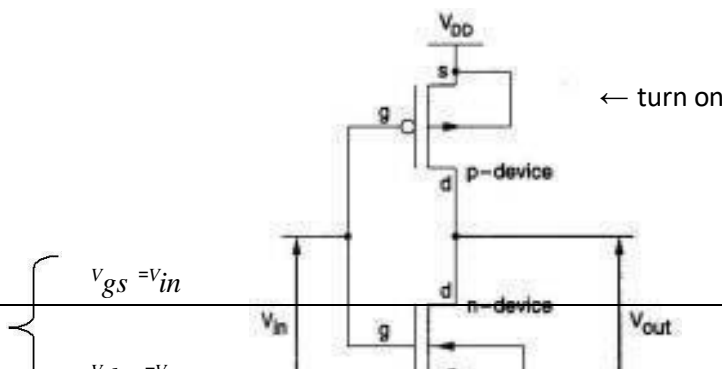
Wire scaling

More uncertainty than transistor scaling

- Many options with complex trade-offs
- For each metal layer
- Need to set H, TT, TB, e1, e2, conductivity of the metal



CMOS INVERTER



$$V_{gs} = V_g - V_{DD} < -|v_t|$$

$$\Rightarrow V_g < V_{DD} - |v_{tp}|$$

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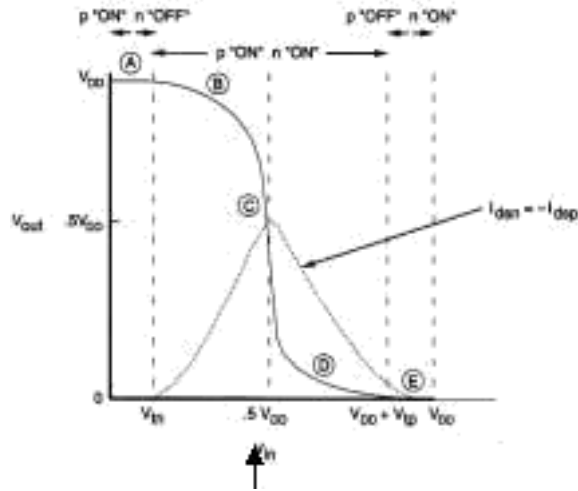


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Both transistors are "on"

$$P = fcv^2 \cdot \alpha$$

↑ (Switching activity)

Solve for

$$\begin{cases} I_{dsn} = -I_{dsp} \\ V_{inn} = V_{inp} \end{cases}$$

(1) Region A.

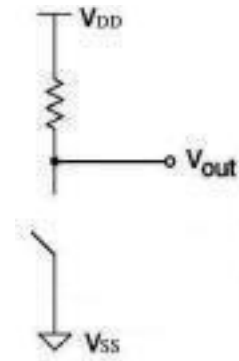
$$0 \leq V_{in} \leq V_{tn}$$

n-device is 'off', $I_{dsn} = 0 (= -I_{dsp})$

p-device is in 'linear' mode

$$V_{out} - V_{DD} = V_{dsp} = 0$$

$$\Rightarrow V_{out} = V_{DD}$$



(2) Region B.

$$V_{tn} \leq V_{in} \leq V_{DD}$$

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2'

p-device : linear mode
n-device : saturation mode
 $[V_i - V_t]^2$

$\mu \epsilon W$

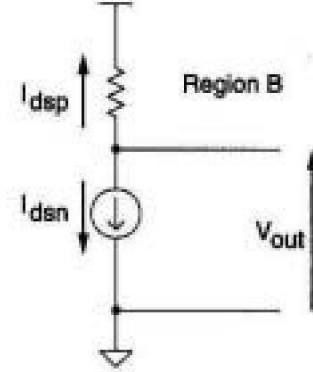
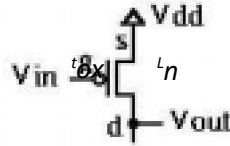
$\frac{n}{n}$

$\frac{n}{n}$

n : $I_{dsn} = \beta_n$

, $\beta_n =$ ()

$\left\{ \begin{array}{l} 2 \end{array} \right.$



p : $V_{gs} = V_{in} - V_{DD}$

$V_{ds} = V_{out} - V_{DD}$



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(3) Region C.

PMOS, NMOS : saturation

β_p

$$I_{dsp} = - \frac{\beta_p}{2} (V_{in} - V_{DD} - V_{tp})^2$$

β_n

$$I_{dsn} = \frac{\beta_n}{2} (V_{in} - V_{tn})^2$$

with $I_{dsp} = -I_{dsn}$

$$V_{DD} + V_{tp} + V_{tn} \frac{\beta_n}{\beta_p}$$

$$\Rightarrow V_{in} = \frac{V_{DD} + V_{tp} + V_{tn} \frac{\beta_n}{\beta_p}}{1 + \frac{\beta_n}{\beta_p}}$$

$$\Rightarrow \text{by setting } \beta_n = \beta_p \text{ and } V_{tn} = -V_{tp}$$

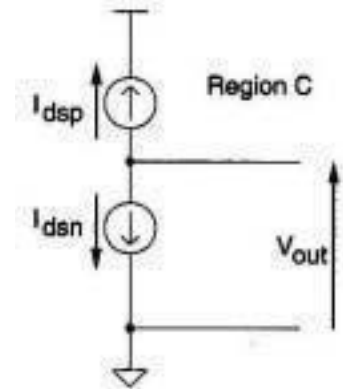
we have

$$\frac{V_{out}}{V_{DD}}$$

: one value only

possible

$$\left\{ \begin{array}{l} V_{out} \\ V_{in} - V_{tn} < V_{out} \end{array} \right.$$



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N-MOS

$$V_{gs} - V_{tn} < V_{ds}$$

$$\begin{aligned} \text{P-MOS} \quad & \left\{ \begin{aligned} (V_{DD} - V_{in}) - V_{tp} &> (V_{DD} - V_{out}) \\ V_{gs} - V_{tp} &> V_{ds} \\ \Rightarrow V_{out} &< V_{in} - V_{tp} \end{aligned} \right. \end{aligned}$$

\Rightarrow

$$V_{in} - V_{tn} < V_{out} < V_{in} - V_{tp}$$

Negative value

$\Rightarrow V_{in}$ is fixed at V_{DD} , V_{out} varies

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N-MOS : linear mode

$$I_{dsp} = -\beta_p (V_{in} - V_{DD} - V_{tp})^2$$

$$V_{out}$$

$$I_{dsn}$$

$$I_{dsn} = \beta_n [(V_{in} - V_{tn}) V_{out} - \frac{V_{out}^2}{2}]$$

$$\text{solve } I_{dsn} = -I_{dsp}$$

$$\Rightarrow V_{out} = (V_{in} - V_{tn}) - \sqrt{\frac{(V_{in} - V_{tn})^2 - \beta_p (V_{in} - V_{DD} - V_{tp})^2}{\beta_n}}$$

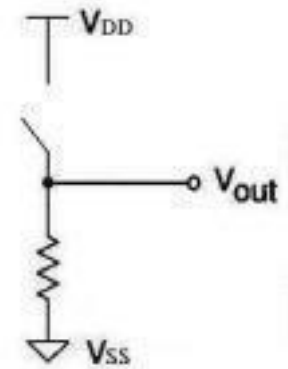
(4) Region E.

$$V_{in} \geq V_{DD} + V_{tp}$$

→ p-device 'off' (n-device is in 'linear' mode)

$$\rightarrow I_{dsp} = 0 \Rightarrow I_{dsn} = 0 \Rightarrow V_{out} = 0$$

see Table 2.3 for summary



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LAYOUT DESIGN RULES

Why we need design rules

- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Layers

Metal (BLUE)

Polysilicon (RED)

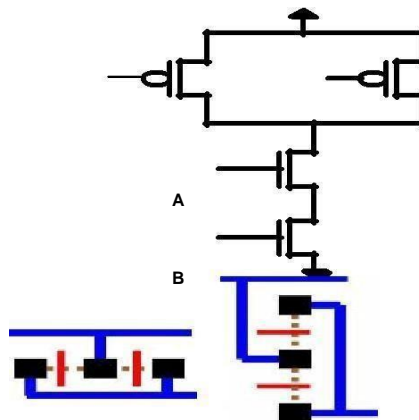
N-Diffusion (Green)

P -Diffusion (Brown)

Contact / Via

Connection Rules

	poly	n-diff	p-diff	metal
poly	S	N	P	NC
n-diff		S	X	NC
p-diff			S	NC
metal				S





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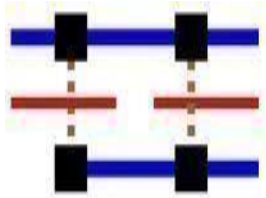
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A

B



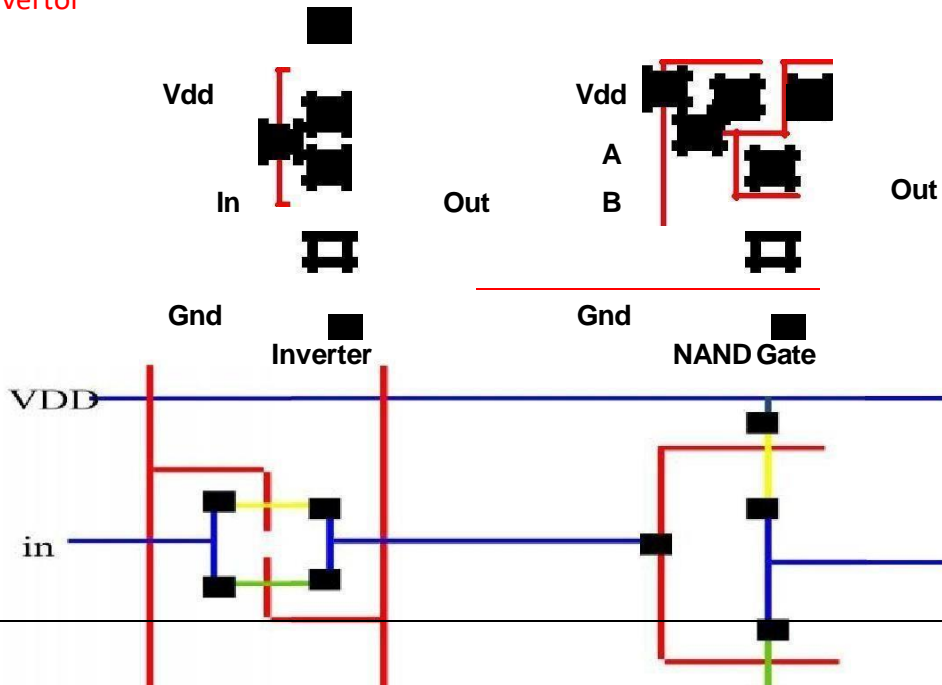
Alternatives - Pull-up Network

Pull-Down Network
(The easy part!)

Complete Stick Diagram

NOR Gate

CMOS
Inverter





Pooja Dr. Sharnbasappa Appaji
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President of Sharnbasveshwar Vidya Vardhak Sangha
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Malkajgiri, Tel. Pooja Appaji
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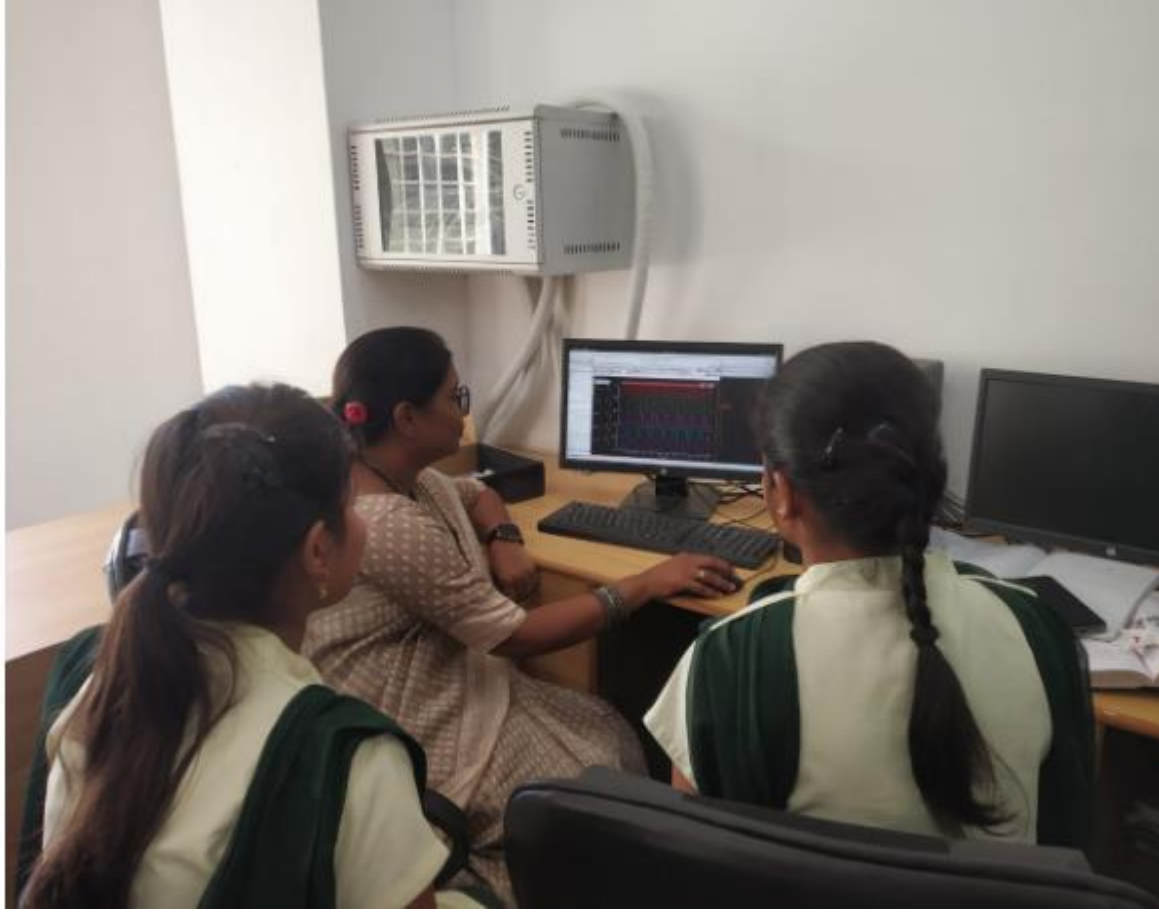
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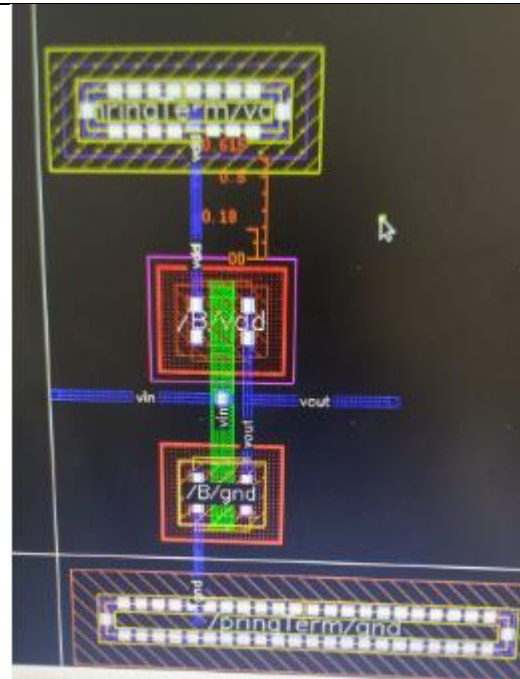
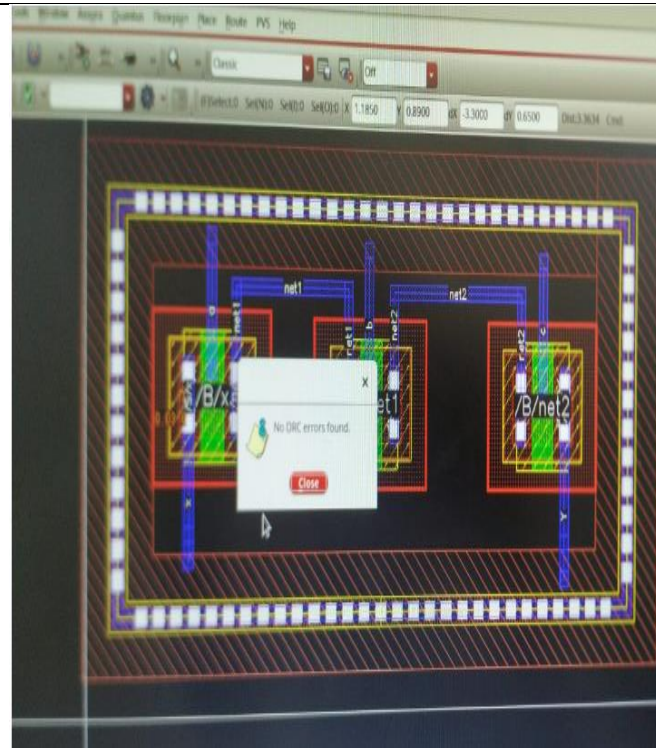
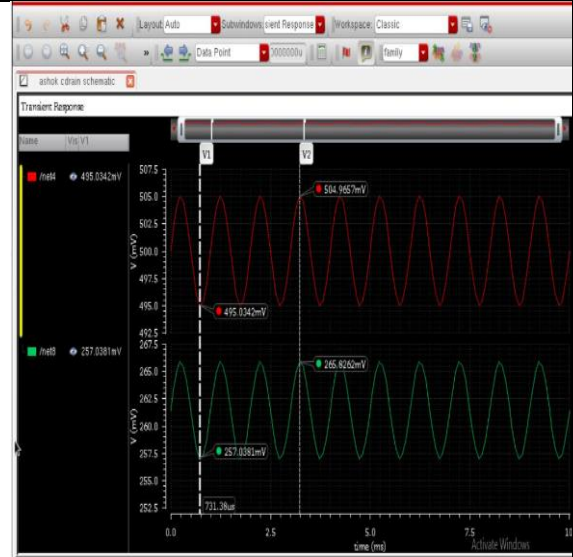
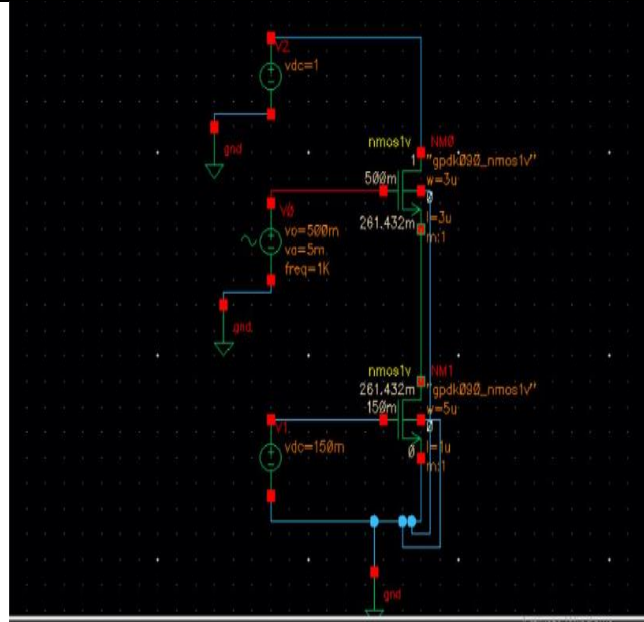
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Centenary Celebrated Sharnbasveshwar Vidya Vardhaka Sangha's

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Pooja Doudappa Appa
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FACULTY OF ENGINEERING & TECHNOLOGY (CO-ED)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
(UNDER IQAC INITIATIVE)

CERTIFICATE

OF ACHIEVEMENT

has successfully completed 12 - weeks value added programme on
"INTRODUCTION TO CIRCUIT AND LAYOUT DESIGN" from 28
April 2023 to 09 July 2023.

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DEPT. ECE
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28/4/23		
1) Lakshi	SG20ECE074 ✓	Subdail
2) Radhika	SG20ECE071 ✓	Prin
3. Shradddha.R.P	SG20ECE081 ✓	SH
4) Pathan Shaheda	SG20ECE064 ✓	Talika
5) Shivani S.C	SG20ECE078 ✓	B
6) Supriya Sunkad	SG20ECE092 ✓	Prin
7) Sen20ECE067	SG20ECE063 ✓	Prin
8) Tyoti.B.R		
9) Dakshayani	SG20ECE051 ✓	Prin
10) Bhargavi	SG20ECE025 ✓	Doodappa
11) Gecda	SG20ECE039 ✓	Prin
12) Bhoomika	SG20ECE028 ✓	B
13) Akanksha	SG20ECE015 ✓	Ramesh
14) ARUN	SG20ECE021 ✓	Prin
15) Anand Manaji	SG20ECE017 ✓	Prin
16) Dupak. Ankad	SG20ECE032 ✓	Prin
17) Abdul Rahman	SG20ECE002 ✓	Prin
18) Adil Khan	SG20ECE001 ✓	Prin
19) Mallikarjun	SG20ECE052 ✓	Prin
20) Niranjan	SG20ECE062 ✓	Prin
21) Ulas	SG20ECE095 ✓	Prin
22) Sudeep .EKLOR	SG20ECE089 ✓	Prin
23) Renuka Singh	SG20ECE072 ✓	Prin
24) Karan Kumar	SG21ELE506 ✓	Prin
25) Ruadeepkumary	SG20ECE067 ✓	Prin
26) Ruadeep Patil	SG20ECE066 ✓	Prin
27) Sannidhi	SG20ECE073 ✓	Prin



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Name	USN	29-04-23
1) Mahesh	SG20ECE050	SG20
2) Samidhi	SG20ECE073	mal
3) Rahul Singh	SG20ECE072	SG20
4) Shradddha R.P	SG20ECE081	SG20
5) Sakshi	SG20ECE074	SG20
6) Shivani S.C.	SG20ECE078	SG20
7) Radhika	SG20ECE071	SG20
8) Supriya	SG20ECE092	SG20
9) Anshana	SG20ECE020	SG20
10) Jyoti	SG20ECE043	SG20
11) Dakshayani S. Math	SG20ECE031	SG20
12) Bhavika D	SG20ECE022	SG20
13) Akanksha	SG20ECE015	SG20
14) Bhargavi	SG20ECE025	SG20
15) Geeta	SG20ECE089	SG20
16) Mahesh Ladvanthi	SG20ECE051	SG20
17) Vidhyanagar Nageshelli	SG20ECE099	SG20
18) Anand	SG20ECE001	SG20
19) Nani Kantar	SG20ECE009	SG20
20) Arjun	SG20ECE021	SG20
21) Anand M	SG20ECE017	SG20
22) Prashant	SG20ECE009	SG20
23) Abhishek Anand	SG20ECE005	SG20
24) Deepak Anand	SG20ECE022	SG20
25) Adil Khan	SG20ECE001	SG20
26) Pradeep patil	SG20ECE066	SG20
27) Pradeep Kumar	SG20ECE067	SG20
28) Mallikarjun	SG20ECE052	SG20
29) Niranjana	SG20ECE062	SG20
30) Umas. Hingundar	SG20ECE095	SG20
31) Sudip Ekhor	SG20ECE089	SG20
32) Karan Kumar	SG20ECE006	SG20
33) Sharan Kumar	SG20ECE076	SG20
34) Pradeep N.D	SG20ECE068	SG20



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Dakshayini	SG20ECE031	30/4/22
Alexandra	SG20ECE020	
Mahesh	SG20ECE050	Ashwini
Pooshanath	SG21ECE509	maah
Manojanath	SG21ECE507	Shanath
Niranjan	SG20ECE062	mykara
Adil Khan	SG20ECE001	Kanchan
Abdul hakim	SG20ECE002	adil
Sannidhi	SG20ECE072	adil
ARUN	SG20ECE021	adil
Anand. Manaji	SG20ECE047	Anand
Deepak Datt	SG20ECE032	Deep
Rahul Singh	SG20ECE072	Rahul
Puadeep. N.R	SG20ECE068	Puadeep
Shashir. Choudhary	SG20ECE076	Shashir
Nagraj	SG20ECE058	Nagraj
Zohab Khan	SG21ECE508	Zohab
Anand	SG21ECE501	Anand
Vidya Prasad Nagaswamy	SG20ECE099	Vidya
Puadeep. Padil	SG20ECE066	Puadeep
Mubashir	SG20ECE057	Mubashir
Mahesh. Lad. Vanti	SG20ECE051	Mahesh
Puadeep. Kumar	SG20ECE017	Puadeep
Raman Kumar	SG21ECE506	Raman
Sudeep. EKLOOR	SG20ECE089	Sudeep
Supriya. Sunkad	SG20ECE092	Supriya
Shraddha. R.P	SG20ECE081	Shraddha
Radhika. B. S	SG20ECE071	Radhika
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1. Shradha, R.P	SG20ECE081	SH
2. Sakshi	SG20ECE074	Sakshi
3. Shisani, S.C	SG20ECE078	Shisani
4. Shaheda.	SG20ECE064	Shaheda
5. Sudeep EKLOOR	SG20ECE089	Sudeep
6. Ullas, H	SG20ECE095	Ullas
7. Karan Kumar	SG21ECE506	Karan
8. Pradeep N.O	SG20ECE068	Pradeep
9. ARUN	SG20ECE021	ARUN
10. Anand	SG20ECE017	Anand
11. Deepak	SG20ECE031	Deepak
12. Bhoomika	SG20ECE028	Bhoomika
13. Akanksha	SG20ECE015	Akanksha
14. Abhishek, Alagi	SG20ECE005	Abhishek
15. Manikanth	SG21EFE507	Manikanth
16. Shashankumar	SG20FCE036	Shashankumar
17. Randeep, Patil	SG20FCE066	Randeep
18. Nagraj	SG20FCE058	Nagraj
19. Mahesh	SG20FCE050	Mahesh
20. Pradeep Kumar	SG20FCE067	Pradeep
21. Aban Rahman	SG20ECE001	Aban Rahman
22. Adil Khan	SG20ECE002	Adil Khan
23. Aushana	SG20ECE020	Aushana
24. Dakshayini	SG20FCE031	Dakshayini
25. Rahul	SG20FCE042	Rahul
26. Sanidhi	SG20FCE073	Sanidhi
27) Mahesh hadiyah	SG20BCE051	Mahesh

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1. Harshvardhan Garkwad	SG20ECE041	A
2. Adil Khan	SG20ECE001	A
3. Deepak	SG20ECE032	(A)
4. Abhishek Allagi	SG20ECE005	B
5. Anand. Marji	SG20ECE017	A
6. Bhoomi Ka	SG20ECE028	B
7. Akanksha	SG20ECE015	(A)
8. Jyoti	SG20ECE043	(A)
9. Anradha	SG20ECE031	A
10. Sakshi	074	S
11. Shirani	078	S
12. Radhika	074	A
13. Shaheda.	064	B
14. Supriya.	092	S
15. Bhargav	SG20ECE020	B
16. Greta	SG20ECE039	(A)
17. Archana	SG20ECE020	(A)
18. Dakshini	SG20ECE031	(A)
19. Sanidhi	SG20ECE073	(A)
20. ARUN	SG20ECE021	(A)
21. Abdul Rahman	SG20ECE002	(A)
22. Rahul Singh	SG20ECE072	(A)
23. Manasak	SG20ECE057	(A)
24. Nagash	SG20ECE058	(A)
25. Vipraj	SG20ECE062	(A)
26. Pradeep Patel	SG20ECE066	(A)
27. Sudip EKLOOR	SG20ECE089	(A)
28. Karan Kumar	SG20ECE06	(A)



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7/5/23

1) Akanksha	SG20ECE015	Pankha
2) Bhavisha Desai	SG20ECE028	Ranika
3) Radhika	SG20ECE091	Rajini
4) Supriya	SG20ECE032	Rajni
5) Shradha R.P	SG20ECE081	Rajni
6) Sakshi	SG20ECE074	Rajni
7) Shivani	SG20ECE078	Rajni
8) Shahela	SG20ECE064	Rajni
9) Anusha	SG20ECE020	Rajni
10) Dakshayani	SG20ECE081	Rajni
11) Adil Khan	SG20ECE001	Rajni
12) ARUN	SG20ECE021	Rajni
13) Anand Manoj	SG20ECE017	Rajni
14) Abhishek Atla	SG20ECE005	Rajni
15) Mahesh Ladva	SG20ECE051	Rajni
16) Karan	SG21ECE506	Rajni
17) Sudeep Eklo	SG20ECE089	Rajni
18) Md. Mubarak	SG20ECE059	Rajni
19) Rajni	SG20ECE058	Rajni
20) Pradeep	SG20ECE066	Rajni
21) Nishanjan	SG20ECE062	Rajni
22) Rahul Singh	SG20ECE072	Rajni
23) S. Sumanth	SG20ECE073	Rajni
24) Aadil Khan	SG20ECE001	Rajni
25) Abdul Rahman	SG20ECE002	Rajni
26) Anand	SG21ECE501	Rajni
27) Mani Kantu	SG21ECE509	Rajni

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9/5/2023		
1) Poojeep kumar	SG20ECE067	Py
2) Adil Khan	SG20ECE001	st
3) Abqur Rahman	SG20ECE002	Abqur
4) Akshithi	SG20ECE074	akshithi
5) Shivani	SG20ECE078	a
6) Pothan Phahesh	SG20ECE064	Waffay
7) Shreya Sunkad	SG20ECE092	Shreya
8) Radhika	SG20ECE071	Radhika
9) Bhoomika	SG20ECE028	Bhoomika
10) Akanksha	SG20ECE015	Akanksha
11) Nagana	SG20ECE058	a
12) Karan Kumar	SG20ECE056	Karan
13) Prashanth	SG20ECE099	Prashanth
14) Suresh Kumar	SG20ECE091	Suresh
15) ARUN	SG20ECE021	ARUN
16) Anand	SG20ECE017	Anand
17) Rohini Singh	SG20ECE072	Rohini
18) Sannidhi	SG20ECE073	Sannidhi
19) Mallikarjun	SG20ECE052	Mallikarjun
20) Anshora	SG20ECE020	Anshora
21) Tyoti	SG20ECE043	Tyoti
22) Vidhansagar Nagaraj	SG20ECE099	Vidhansagar
23) Poojeep	SG20ECE066	Poojeep
24) Mahesh	SG20ECE050	Mahesh
25) Anand	SG20ECE051	Anand
26) Manikant	SG20ECE057	Manikant
27) Sudeep Eklor	SG20ECE089	Sudeep
28) Mahesh Ladvantur	SG20ECE051	Mahesh
29) Alshishet. Allogi	SG20ECE005	Alshishet

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24/5/23

1) Akanksha	SG20FCE015	Panksha
2) Bhoomika Dasa	SG20FCE028	Boonika
3) Gita	SG20FCE033	Gita H.P
4) Supriya Sunkat	SG20FCE092	Supriya
5) Radhika	SG20FCE071	Radhika
6) Shradha R.P	SG20FCE081	Shradha
7) Sakshi	SG20FCE074	Sakshi
8) Shahida	SG20FCE064	Shahida
9) Shivani S.C	SG20FCE078	Shivani
10) Abdul Khan	SG20FCE001	Abdul Khan
11) Abdul Kader	SG20FCE002	Abdul Kader
12) Rahul Singh	SG20FCE072	Rahul Singh
13) Prashanth	SG20FCE009	Prashanth
14) Anand	SG20FCE051	Anand
15) Pradeep	SG20FCE066	Pradeep
16) Garenkumar	SG20FCE016	Garenkumar
17) Sudeep Ekloa	SG20FCE089	Sudeep Ekloa
18) Karan Kumar	SG20FCE050	Karan Kumar
19) Nagesh	SG20FCE058	Nagesh
20) Harshvardhan	SG20FCE091	Harshvardhan
21) Vidyaasagar	SG20FCE099	Vidyaasagar
22) Nisanjan	SG20FCE062	Nisanjan
23) Natesh	SG20FCE050	Natesh
24) Sannidhi	SG20FCE073	Sannidhi



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1) Akanksha	SG20ECE015	Ankha
2) Shoenka	SG20ECE028	Bumika
3) Supriya	SG20ECE092	Supriya
4) Radhika	SG20ECE071	Radhika
5) Sakshi	SG20ECE074	Sakshi
6) Shradha	SG20ECE081	Shradha
7) Bhargavi	SG20ECE025	Bhargavi
8) Geeta	SG20ECE039	Geeta
9) Suchana	SG20ECE020	Suchana
10) Adil Khan	SG20ECE001	Adil
11) Arund	SG21ECE501	Arund
12) Prashanth	SG21ECE509	Prashanth
13) Rahul Singh	SG20ECE072	Rahul
14) Nagendra	SG20ECE058	Nagendra
15) Sannishi Kulkarni	SG20ECE073	Sannishi
16) Karan Kumar	SG21ECE506	Karan
17) Vilas Hiragauda	SG20ECE095	Vilas
18) Sudeep Ekka	SG20ECE089	Sudeep
19) Anand Manaji	SG20ECE017	Anand
20) Abhishek Allagi	SG20ECE005	Abhishek
21) Sharankumar C	SG20ECE076	Sharankumar



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