### CHOICE BASED CREDIT SYSTEM (CBCS) SCHEME SCHEME OF TEACHING & EXAMINATION 2017-2018 M.Tech: <u>DIGITAL COMMUNICATION & NETWORKING</u>

#### Semester : I

S h i 4	Name of the Subject	Teaching &Learning(hours/week)		Practical/	Duration	Marks for		<b>T</b> ( )	
Code		Lecture	Discourse/ Self Study/ Assignment	Field Work	of Exam in Hours	CIE	SEE	1 otai Marks	CREDITS
17LDE11	Advanced Engineering Mathematics	3	3	-	3	50	50	100	4
17LDN12	Antenna Theory and Design	3	3	-	3	50	50	100	4
17LVE13	Advanced Embedded System	3	3	-	3	50	50	100	4
17LDN14	Advanced Digital Communications	3	3	-	3	50	50	100	4
17LXX15X	Elective-1	3	3	-	3	50	50	100	4
17LDNL16	Advanced Communication Lab	-	-	6	3	50	50	100	2
17LDN17	Project-1	-	-	6	3	50	50	100	2
	Total	15	15	12		350	350	700	24

Electives-1	
17LDN151	Advanced Computer Networks
17LDN152	Optical Communication & Networking
17LDE153	ASIC
17LVE154	Advanced Computer Architecture.
17LDN155	Multimedia Over Communication links

### CHOICE BASED CREDIT SYSTEM (CBCS) SCHEME SCHEME OF TEACHING & EXAMINATION 2017-2018 M.Tech: DIGITAL COMMUNICATION & NETWORKING

#### Semester: II

Subject Code	Name of the Subject	Teaching &Learning(hours/week)		Practical/	Duration	Marks for		Tatal	
		Lecture	Discourse/ Self Study/ Assignment	Field Work	of Exam in Hours	CIE	SEE	Marks	CREDITS
17LDE21	Advanced DSP	3	3	-	3	50	50	100	4
17LDE22	Error Control Coding	3	3	-	3	50	50	100	4
17LDN23	Wireless Communication	3	3	-	3	50	50	100	4
17LDN24	RF and Microwave Circuit Design	3	3	-	3	50	50	100	4
17LXX25X	Elective-2	3	3	-	3	50	50	100	4
17LDNL26	Advanced DSP Lab	-	-	6	3	50	50	100	2
17LDN27	Project-2	-	-	6	3	50	50	100	2
	Total	15	15	12	-	350	350	700	24

Electives-2	
17LDN251	Wireless Mobile Networks
17LDE252	MEMS
17LDN253	Wireless Sensor Networks
17LDN254	Cryptography and Network Security
17LVE255	VLSI Design for Signal Processing

### CHOICE BASED CREDIT SYSTEM (CBCS) SCHEME SCHEME OF TEACHING & EXAMINATION 2017-2018 M.Tech: <u>DIGITAL COMMUNICATION & NETWORKING</u>

Semester : III

Subject	Name of the Subject	Teaching &Learning(hours/week)		Practical/	Duration	Marks for		Total	
Code		Lecture	Discourse/ Self Study/ Assignment	Field Work	of Exam in Hours	CIE	SEE	Marks	CREDITS
17LDN31	Internship	-	-	40	03	50	50	25	20
17LDN32	Main Project Phase -1	-	-	2	-	50	-	50	01
	Total	-	-	-	-	100	50	150	21

#### Note: Internship comprises following sub components:

- 1. Presentation on Internship(after 8 weeks from the date of commencement)(CIE) for 25Marks
- 2. Evaluation of Internship Report(CIE for 25Marks)

Viva-Voce on Internship (SEE) for 50Marks

### CHOICE BASED CREDIT SYSTEM (CBCS) SCHEME SCHEME OF TEACHING & EXAMINATION 2017-2018 M.Tech: <u>DIGITAL COMMUNICATION & NETWORKING</u>

#### **SEMESTER: IV**

Subject	Nome of the	T &Learnin	eaching ng(hours/week)	Practical/	Duration	Marks for		Total	
Code	Subject	Lecture	Discourse/ Self Study/ Assignment	Field Work	of Exam in Hours	CIE	SEE	Marks	CREDITS
17LDN41	Wireless Broadband Communications	3	3	-	3	50	50	100	4
17LXX42X	Elective-3	3	3	-	3	50	50	100	4
17LDN43	Evaluation of Project Phase -2	-	-	24	3	100	200	300	12
	Total	6	6			200	300	500	20

Elective-3	
17LVE421	CMOS RF Circuit Design
17LDN422	Advances in Image Processing
17LDN423	Communication System Design using DSP Algorithms
17LDE424	Reconfigurable Computing
17LDE425	Advanced Microcontrollers

Note:

- 1. **Project Phase-1**: 6-week duration shall be carried out between IInd and IIIrd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.
- 2. **Project Phase-II**: 16-week duration during IVth semester. CIE 100marks evaluation done by the committee constituted comprising of Chairman of the department, Guide and Senior faculty of the department.
- 3. Main Project Evaluation and Viva-Voce: Evaluation shall be taken up at the end of IVth semester.
  - a. Internal Examiner shall carry out the evaluation for 100 marks.
  - b. External Examiner shall carry out the evaluation for 100 marks.
  - c. The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.
  - d. Viva-Voce examination of the project work shall be conducted jointly by internal and external examiner for 100 Marks.

## **ADVANCED ENGINEERING MATHEMATICS**

As per choice based credit system(CBCS)scheme Semester – I					
Subject Code	17LDE11	CIE	50		
Number of Lecture Hours/Week	03	SEE	50		
Total Number of Lecture Hours	48	Exam hours	3Hrs		

### Credits : 04

- Acquaint with principles of linear algebra, calculus of variations, probability theory and random process.
- Apply the knowledge of linear algebra, calculus of variations, probability theory and random process in the applications of electronics and communication engineering sciences.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Linear Algebra		
Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank- Nullity theorem (without proof). Gaussian Elimination Matrix form of linear transformations-Illustrative examples.	10Hrs	L1, L2
Module – 2 : Linear Algebra-II		
Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. Diagonalization Method QR decomposition, singular value decomposition, least square approximations.	10 Hours (Text 1 & Ref. 1)	L1,L2
Module – 3: Calculus of Variations		
Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. Module – 4 : Probability Theory	10 Hours (Text 2 & Ref. 2)	L1,L2
Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment	10 Hours (Text 3 & Ref. 3)	L1,L2

generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.		
Module – 5 : Joint probability distributions		
Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples. Random process- Classification, stationary and Ergodic random process. Auto correlation function-properties, Gaussian random process. Poisson Process, Binomial Process	10 Hours (Text 3 & Ref. 3)	L1, L2

- a. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- b. Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
- c. Utilize the concepts of functionals and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
- d. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
- e. Apply the idea of joint probability distributions and the role of parameter dependent random variables in random process.

### **Text Books**:

- 1. David C.Lay, Steven R. Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
- 2. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.
- 3. Scott L.Miller, DonaldG. Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition,2013.

### **Reference books:**

- 1. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
- 2. Elsgolts, L.:"Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
- 3. T.Veerarajan: "Probability, Statistics and Random Process", 3rd Edition, Tata McGraw Hill Co.,2008.

### Web links:

- 1. http://nptel.ac.in/courses.php?disciplineId=111
- 2. http://www.class-central.com/subject/math(MOOCs)
- 3. http://ocw.mit.edu/courses/mathematics/
- 4. www.wolfram.com

## **ANTENNA THEORY AND DESIGN**

As per choice based credit system(CBCS)scheme Semester – I					
Subject Code	17LDN12	CIE	50		
Number of Lecture Hours/Week	03	SEE	50		
Total Number of Lecture Hours	48	Exam hours	3Hrs		

#### Credit:04

- a. Introduce and discuss different types of Antennas, various terminologies, excitations.
- b. Study different types of Arrays, Pattern-multiplication, Feeding techniques.
- c. Calculate gain of aperture antennas, Reflector antennas and analyze general feed model.
- d. Define, describe, and illustrate principle behind antenna synthesis.
- e. Introduction of Method of moments, Pocklington's integral equation, Source modeling.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Antenna Fundamentals and Definitions		
Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization	10Hrs	L1, L2
Module – 2 : Arrays & Antenna Synthesis		
Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Non-uniformly excited equally spaced linear arrays, Mutual coupling. Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.	10Hrs	L1,L2,L3,L4,L5
Module – 3: Resonant Antennas & Broadband antennas:		
Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro- strip antenna. Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas.	10 Hrs	L1,L2
Module – 4 : Aperture antennas		
Techniques for evaluating gain, Reflector antennas- Parabolic	10 Hrs	L1,L2,L3,L5

reflector antenna principles, Axi-symmetric parabolic reflector antenna, Offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.		
Module – 5 : Methods of Moments & Smart Antennas		
Introduction to methods of moments, Pocklington's Integrals		
equation and Kirchoff Networking equation.	10 Hrs	L1, L2
Smart Antennas, Multiple Input Multi Output Systems		

- a. Classify different types of antennas
- b. Define and illustrate various types of array antennas
- c. Design antennas like Yagi-Uda, Helical antennas and other broad band antennas
- d. Describe different antenna synthesis methods. Apply methods like MOM

### **Text Book:**

- 1. Stutzman and Thiele, "Antenna Theory and Design", 2nd Edition, John Wiley, 2010.
- 2. Andreas Molisch, 'Wireless Communication'. 2nd Edition, John Wiley.

- 1. C. A. Balanis, "Antenna Theory Analysis and Design", John Wiley, 2nd Edition 2007.
- 2. J. D. Krauss, "Antennas and Wave Propagation", McGraw Hill TMH, 4th Edition, 2010.
- 3. A.R.Harish, M.Sachidanada, "Antennas and propagation", Pearson Education, 2015.

## **ADVANCED EMBEDDED SYSTEM**

As per choice based credit system(CBCS)scheme			
	Semester -	=1	
Subject Code	17LVE13	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- a. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- b. Describe the hardware software co-design and firmware design approaches
- c. Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- d. Program ARM CORTEX M3 using the various instructions, for different applications.

Modules		Revised Bloom's Taxonomy(RBT) Level
Module-1 : Embedded System		
Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	10Hrs	L1, L2, L3
Module – 2 : Hardware Software Co-Design		
embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13)	10 Hrs	L1, L2, L3, L4
Module – 3: ARM-32 bit Microcontroller		
Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	10 Hrs	L1, L2. L3
Module – 4 : Instruction Sets		-
Assembly basics, Instruction list and description, useful	10 Hrs	L1, L2, L3, L4

instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6)		
Module – 5 : Exceptions		
Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10)	10 Hrs	L1, L2, L3

- a. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- b. Explain the hardware software co-design and firmware design approaches.
- c. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- d. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

### **Text Books:**

- 1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
- 2. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd edn, Newnes, (Elsevier), 2010.

### **Reference Book:**

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

## **ADVANCED DIGITAL COMMUNICATION**

As per choice based credit system(CBCS)scheme			
Semester – I			
Subject Code	17LDN14	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credit:04

- a. Analyze the operation of different modulation techniques and analyze the error performance of digital modulation techniques in presence of AWGN noise.
- b. Explain and demonstrate the model of discrete time channel with ISI.
- c. Explain the model of discrete time channel by equalizer.
- d. Explain various types of equalizers used for channel modeling and adjusting the filter coefficients
- e. Understand the concept of spread spectrum communication system and analyze the error performance.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Digital Modulation Schemes			
Representation of Digitally Modulated Signals, Memory less Modulation Methods-PAM, Phase Modulation, QAM, Multidimensional Signalling, Signalling Schemes with memory: CPFSK, CPM, MSK, OQPSK. Transmit PSD for Modulation Schemes (Chapter 3: 3.1, 3.2, 3.3, 3.4.1 and 3.4.2 of Text)	10Hrs	L1, L2, L3, L4	
Module – 2 : Optimum Receivers for AWGN channels			
Waveform and Vector channel models, Waveform and Vector AWGN channels- Optimal detection, Implementation, Optimal Detection and Error Probability for Band limited signaling, Optimal detection and error probability for power limited signaling. Non Coherent Detection (without derivations(Chapter 4: 4.1, 4.2 - 4.2.1, 4.2.2, 4.3, 4.4, 4.5.1, 4.5.2, eqn 4.5.45 to 4.5.47, 4.5.5 upto eqn 4.5.62 of Text)	10 Hours	L1, L2, L3, L4	
Module – 3: Multichannel and Multicarrier Signalling & Synchronization			
Multichannel Communications in an AWGN channel, Multicarrier Communications in AWGN channel (Chapter 11- 11.1, 11.2- 1 to 11.2-5 of Text). Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery (Chapter 5- 5.1 to 5.3, of Text).	10 Hours	L2, L3, L4	
Module – 4 : Digital Communication through band-limited channels & Adaptive equalization			

Characterization of Band-limited channels, Optimum Receiver for channels with ISI and AWGN, Linear equalization, Decision feedback equalization (Chapter 9: 9.1,9.3- 9.3.1, 9.3.2, 9.4- 9.4.1, 9.4.2, 9.4.4, 9.4.5, 9.5- 9.5.1, 9.5.3 of Text). Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive equalization of Trellis - coded signals (Chapter 10: 10.1, 10.2, 10.3 of Text).	10 Hours	L1, L2, L3, L4
Module – 5 : Spread spectrum signals for digital communication		
Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, Frequency hopped spread spectrum signals, CDMA, Time hopping SS, Synchronization of SS systems (Chapter 12 of Text).	10 Hours	L1, L2

### **Course Outcomes:**

After studying this course, students will be able to:

- 1. Acquire knowledge of A
  - a. Advanced topics on digital communication.
  - b. Application and practical implementation of various Digital Modulation techniques.
  - c. Inter symbol interference (ISI ) and its channel modeling .
  - d. Different types spread spectrum system
  - e. Different filtering algorithms for the ISI elimination
  - f. The effect of signal characteristics on the choice of a channel model.
- 2. Analyze the performance of
  - a. Digital Modulation techniques.
  - b. Different filtering algorithms.
  - c. Spread spectrum communication system

#### **Text Books:**

1. John G. Proakis, Masoud Salehi, "Digital Communications", McGraw Hill, 5th Edition, 2008.

#### **Reference: Book:**

1. Bernard Sklar, "Digital Communication - Fundamental and applications", Pearson education (Asia), Pvt. Ltd., 2nd edition, 2001.

## ADVANCED COMPUTER NETWORKS

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LDN151	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- a. Develop an awareness towards basic networking principles
- b. Learn various aspects involved in multiple access and multiplexing
- c. Develop an awareness regarding the LAN architectures and the various data switching techniques
- d. Learn the scheduling techniques of networks
- e. Learn protocols operating in at different layers of computer networks
- f. Develop an awareness towards the network control and traffic management

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction to networks & Multiple Access			
Computer network, Telephone networks, Networking principles (Text 1), Protocol layering (Text 2), Multiplexing- TDM, FDM, SM, WDM (Text 1). Introduction, Choices and constraints, base technologies, centralized and distributed access schemes (Text 2).	10Hrs	L1, L2, L3, L4	
Module – 2 : Local Area Networks & Scheduling			
Ethernet-Physical layer, MAC, LLC, LAN interconnection, Token ring- Physical layer, MAC, LLC, FDDI (Text 1). Switching- introduction, circuit switching, packet switching, multicasting (Text 2). Introduction, requirements, choices, performance bounds, best- effort techniques. Naming and addressing (Text 2).	10 Hours	L1, L2, L3, L4	
Module – 3: SONET & Internet protocols-			
<ul><li>SONET, SDH (Text 2), ATM Networks- features, signaling and routing, header and adaptation layers (Text 1), virtual circuits, SSCOP, Internet- addressing, routing, end point control (Text 2).</li><li>IP, TCP, UDP, ICMP, HTTP (Text 2).</li></ul>	10 Hours	L2, L3, L4	
Module – 4 : Traffic Management			
Introduction, framework for traffic management, traffic models,	10 Hours	L1, L2, L3, L4	

traffic classes, traffic scheduling (Text 2).				
Module – 5 : Control of Networks & Congestion and flow control				
Objectives and methods of control, routing optimization in				
circuit and datagram networks, Markov chains, Queuing models				
in circuit and datagram networks (Text 1).		1112		
Window congestion control, rate congestion control, control in	10 11001 5	11, 12		
ATM Networks (Text 1), flow control model, open loop flow				
control, closed loop flow control (Text 2).				

- 1. Choose
  - a. appropriate multiple access and multiplexing techniques as per the requirement.
  - b. standards for establishing a computer network
  - c. switching techniques based on the applications of the network
  - d. IP configuration for the network with suitable routing, scheduling, error control and flow control
- 2. Analyze and develop various network traffic management and control techniques

### **Text Books:**

- 1. J. Walrand and P. Varaya, "High performance communication networks", Harcourt Asia (Morgan Kaufmann), 2000.
- 2. S. Keshav, "An Engineering approach to Computer Networking", Pearson Education, 1997.

- 1. Leon-Garcia, and I. Widjaja, "Communication network: Fundamental concepts and key architectures", TMH, 2000.
- 2. J. F. Kurose, and K. W. Ross, "Computer networking: A top down approach featuring the Internet", Pearson Education, 2001.

## **OPTICAL COMMUNICATION AND NETWORKING**

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LDN152	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credit:04

- a. Mathematically analyze and conceptualize basics of optical networking and its associated nonlinear artifacts and effects.
- b. Develop awareness regarding optical devices and their working strategies
- c. Develop awareness of WDM principles, and that of power penalty issues existent in optical Networks
- d. Get insight into the design of various types of Lasers and understand the techniques of coherent transmission.
- e. Develop an awareness towards the backbone architectures of optical networking with the present trends in access networks
- f. Design second generation optical networks using various existent & devices like OADM, OLT and OXC and to mathematically model the problems in the design Of WDM networks

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction to optical networking			
Propagation of signals in optical fiber, Different losses,			
Nonlinear effects, Solutions, Optical sources, Detectors.	10Hrs	11121314	
Optical Components (Part-1): Couplers, Isolators, Circulators	101115	L1, L2, L3, L4	
and Multiplexers.			
Module – 2 : Optical Components (Part-2)			
Filters, Gratings, Interferometers, Amplifiers.			
Modulation - Demodulation: Formats, Ideal receivers,	10 Hours	11121314	
Practical detection receivers, Optical preamplifiers, Noise		L1, L2, L3, L4	
considerations, Bit error rates, Coherent detection.			
Module – 3: Transmission System Engineering			
System model, Power penalty, Transmitter, Receiver, Different			
optical amplifiers Client Layers: Client layers of optical layer,			
SONET/SDH, Multiplexing, layers, Frame structure, ATM	10 Hours	L2, L3, L4	
functions, Adaptation layers, Quality of Service (QoS) and flow			
control, ESCON, HIPPI			

Module – 4 : WDM network elements			
Optical line terminal, Optical line amplifiers, Optical Add/ Drop Multiplexors, Optical cross connectors. <b>WDM Network Design</b> : WDM network design, Cost tradeoffs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion.	10 Hours	L1, L2, L3, L4	
Module – 5 : Control and Management			
Network management functions, management framework, Information model, management protocols, Layers within optical layer. <b>Control and Management (Part-2):</b> Performance and fault management, Impact of transparency, BER measurement, Optical trace, Alarm management, Configuration management.	10 Hours	L1, L2	

- a. Recognize and select various optical networking components according to the prescribed design specifications Learn
- b. the aspects of data transmission, loss hindrances and other artifacts
- c. affecting the network operation
- d. the issues involved in setting up and maintenance of access part of optical
- e. network with the latest trends in the data communication
- f. Design a WDM network and study the component and network management
- g. aspects

#### **Text Book:**

1. Rajiv Ramswami and K. N. Sivarajan, "Optical Networks", Morgon Kauffman Publishers, 3rd edition, 2010.

- 1. John M. Senior, "Optical fiber communication", Pearson edition, 2000.
- 2. Gerd Kaiser, "Optical fiber Communication Systems", John Wiley, New York, 1997.
- 3. P. E. Green, "Optical Networks", Prentice Hall, 1994.

## ASIC DESIGN

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LVE153	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit: 04

- a. Explain ASIC methodologies and programmable logic cells to implement a function on IC.
- b. Analyze backend physical design flow, including partitioning, floor planning, and placement and routing.
- c. Gain sufficient theoretical knowledge for carrying out FPGA and ASIC design.
- d. Design CAD algorithms and explain how these concepts interact in ASIC design.

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction to ASICs			
Introduction to ASICs, Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Datapath Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.		L1, L2	
Module – 2 : ASIC Library Design:	-		
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages. Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.	10 Hours	L1-L3	
Module – 3: Programmable ASIC I/O Cells			
<ul> <li>Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.</li> <li>Low-level design entry: Schematic entry: Hierarchical design, Netlist screener.</li> <li>ASIC Construction: Physical Design, CAD Tools.</li> <li>Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.</li> </ul>	10 Hours	L1- L4	
Module – 4 : Dynamic & BiCMOS Logic Circiuts			
Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. <b>BiCMOS Logic Circuits</b> : Introduction, Bipolar Junction	10 Hours	L1, L2, L3, L4	

Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.		
Module – 5 : Chip Input and Output (I/O) Circuits:		
Introduction, ESD Protection, Input Circuits, Output Circuits		
and L(di/dt) Noise, On-Chip Clock Generation and Distribution,		
Latch-Up and Its Prevention.	10 Hours	1213
Design for Manufacturability: Introduction, Process	10 11001 5	L2, L3
Variations, Basic Concepts and Definitions, Design of		
Experiments and Performance Modeling.		

- a. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation..
- b. Analyse the Switching Characteristics in Digital Integrated Circuits.
- c. Use the Dynamic Logic circuits in state of the art VLSI chips.
- d. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
- e. Use Bipolar and Bi-CMOS circuits in very high speed design.

### **Text Book:**

1. Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

- 1. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
- 2. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.

## **ADVANCED COMPUTER ARCHITECTURE**

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LVE154	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credits : 04

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Parallel Computer Models:		
Classification of parallel computers,		
Multiprocessors and multicomputers, Multivector and SIMD		
computers.	10Hrs	121314
Program and Network Properties, Conditions of parallelism,	101115	12, 13, 14
Data and resource Dependences, Hardware and software		
parallelism. (Text 1).		
Module – 2 : Program Patitioning and Scheduling		
Program partitioning and scheduling, Grain Size and latency,		
Program flow mechanisms, Control flow versus data flow, Data		
flow Architecture, Demand driven mechanisms, Comparisons	10 Hound	
of flow mechanisms, Principles of Scalable Performance,	10 Hours	L2, L3, L4
Performance Metrics and Measures, Parallel Processing		
Applications, Speedup Performance Laws, Scalability Analysis		
and Approaches. (Text 1)		
Module – 3: Calculus of Variations		
Advanced Processors: Advanced processor technology,		
Instruction-set Architectures, CISC Scalar Processors, RISC		
Scalar Processors, Superscalar Processors, VLIW Architectures,	10 Hours L1, L2, L3	
Pipelining, Linear pipeline processor, nonlinear pipeline		
processor, Instruction pipeline design.		
(Text 1)		
Module – 4 : Mechanisms for instruction pipelining		
Mechanisms for instruction pipelining, Dynamic instruction	10 17	
scheduling, Branch Handling techniques, branch prediction,	10 Hours L2, L3, L4	
Arithmetic Pipeline		

Design, Computer arithmetic principles, Static Arithmetic		
pipeline, Multifunctional arithmetic pipelines. (Text 1)		
Module – 5 : Multithread and Dataflow Architecture:		
Multithread and Dataflow Architecture: Principles of		
Multithreading, Scalable and Multithreaded Architecture,	10 Hours	111213
Dataflow Architecture, Symmetric shared memory architecture,		L1, L2, L3
distributed shared memory architecture. (Text 1 & 2)		

Course outcomes: At the end of this course, the students will be able to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

### **Text Books:**

1. Kai Hwang, —Advanced computer architecturell, TMH. 2007.

2. Kai Hwang and Zu, -Scalable Parallel Computers Architecturel, MGH, 2008.

### **Reference Books:**

1. M.J. Flynn, —Computer Architecture, Pipelined and Parallel Processor Designl, Narosa Publishing, 2002.

2. D.A.Patterson, J.L.Hennessy, —Computer Architecture: A quantitative approach "Morgan Kauffmann feb,2002

## **MULTIMEDIA OVER COMMUNICATION LINKS**

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LDN155	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- a. Gain fundamental knowledge in understanding the basics of different multimedia networks, applications, media types like text and image.
- b. Analyse media types like audio and video and gain knowledge on multimedia systems.
- c. Analyse Audio compression techniques required to compress Audio.
- d. Analyse compression techniques required to compress video.
- e. Gain fundamental knowledge about the Multimedia Communications in different Networks.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction to Multimedia Communications			
<ul> <li>Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.</li> <li>(Chap. 1 of Text1)</li> <li>Information Representation: Introduction, Text, Images.</li> <li>(Chap. 2- Sections 2.2 and 2.3 of Text 1)</li> </ul>	10Hrs	L1, L2, L3	
Module – 2 : Information Representation			
Audio and Video. (Chap. 2 - Sections 2.4 and 2.5 of Text 1) <b>Distributed multimedia systems</b> : Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems. (Chap. 4 - Sections 4.1 to 4.5 of Text 2	10 Hours	L1, L2, L3	
Module – 3: Multimedia Processing in Communication:			
Introduction, Perceptual coding of digital Audio signals, Transform Audio Coders, Audio Sub band Coders.(Chap. 3 - Sections 3.1, 3.2, 3.6, 3.7 of Text 2)	10 Hours	L2, L3, L4	
Module – 4 : Multimedia Communication Standards			
Introduction, MPEG approach to multimedia standardization,	10 Hours	L1, L2, L3, L4	

MPEG-1, MPEG-2, Overview of MPEG-4. (Chap. 5 - Sections 5.1		
to 5.4 and 5.5.1 of		
Text 2)		
Module – 5 : Multimedia Communication Across Networks		
Packet audio/video in the network environment, Video transport		
across generic networks, Multimedia Transport across ATM	10 Hours	L1, L2
Networks. (Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2)		

- a. Understand basics of different multimedia networks and applications.
- b. Analyze media types like audio and video to represent in digital form.
- c. Understand different compression techniques to compress audio.
- d. Understand different compression techniques to compress audio video.
- e. Describe the basics of Multimedia Communication Across Networks

### **Text Books:**

- 1. Fred Halsall, "Multimedia Communications", Pearson education, 2001, ISBN 9788131709948.
- 2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN - 9788120321458.

### **Reference Books:**

1. Raif steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002, ISBN -9788177584417..

### ADVANCED COMMUNICATION LAB

As per choice based credit system(CBCS)scheme Semester – I			
Laboratory Code	17LDNL16	СЕЕ	50
Number of Lecture		SEE	50
Hours/Week	06	Exam hours	3Hrs

#### Credits :02

**Course objectives:** This laboratory course enables students to get practical experience

- Radiation pattern of antennas.
- Determining gain and directivity of a given antenna.
- Working of Klystron source.
- S-parameters of some microwave passive devices.
  - 1. Matlab/C implementation of to obtain the radiation pattern of an antenna.
  - 2. Study of radiation pattern of different antennas.
  - 3. Determine the directivity and gains of Horn/ Yagi/ dipole/ Parabolic antennas.
  - 4. Impedance measurements of Horn/Yagi/dipole/Parabolic antennas.
  - 5. Study of radiation pattern of E & H plane horns.
  - 6. Significance of Pocklington's integral equation.
  - 7. Study of digital modulation techniques using CD4051 IC.
  - 8. Conduct an experiment for Voice and data multiplexing using optical fiber.
  - 9. Determination of the modes transit time, electronic timing range and sensitivity of Klystron source.
  - 10. Determination of VI characteristics of GUNN diode, and measurement of guide wave length, frequency, and VSWR.
- 11. Determination of coupling coefficient and insertion loss of directional couplers and Magic tree.
- 12. Build a hardware pseudo-random signal source and determine statistics of the generated signal source.

#### **Course Outcomes**

On the completion of this laboratory course, the students will be able to:

- a. Plot the radiation pattern of some antennas using matlab and wave guide setup
- b. Obtain the S-parameters of Magic tee and directional couplers.
- c. Test the IC CD4051 for modulation techniques.
- d. Study multiplexing techniques using OFC kit..

#### **Conduction of Practical Examination:**

All laboratory experiments (nos) are to be included for practical examination. Students are allowed to pick one experiment from each part and execute both Strictly follow the instructions as printed on the cover page of answer script for break up Of Marks

PART –A: Procedure + Conduction + Viva: 10 + 20 + 10 (40)

PART –B: Procedure + Conduction + Viva: 10 + 20 + 10(40)Change of experiment is allowed only once and marks allotted to the procedure part to be made zero.

## **ADVANCED DSP**

As per choice based credit system(CBCS)scheme Semester – II			
Subject Code	17LDE21	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credits : 04

- Understand Multirate digital signal processing principles and its applications.
- Estimate the various spectral components present in the received signal using different spectral estimation methods such as Parametric and Nonparametric.
- Design and implement an optimum adaptive filter using LMS and RLS algorithms.
- Understand the concepts and mathematical representations of Wavelet transforms.

Modules		Revised Bloom's Taxonomy(RBT) Level
Module-1 : Multirate Digital Signal Processing:		
Introduction, decimation by a factor 'D', Interpolation by a factor 'T, sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1)	10Hrs	L1, L2, L3
Module – 2 : Linear prediction and Optimum Linear Filters:		
Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations The Levinson-Durbin Algorithm. Properties of the Linear Prediction- Error Filters. (Text 1)	10 Hours	L1, L2, L3
Module – 3: Adaptive filters: Applications of adaptive filters-		
Adaptive channel equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters- The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm. (Text 1)	10 Hours	L1, L2, L3
Module – 4 : Power Spectrum Estimation:		
Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods. Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters,	10 Hours	L1, L2, L3

Burg Method for the AR Model parameters, Unconstrained least- squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1)		
Module – 5 : Wavelet Transforms:		
The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future. Continuous Wavelet and Short Time Fourier Transform: Wavelet Transform, Mathematical preliminaries, Properties of wavelets. Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2)	10 Hours	L1, L2, L3

- a. Design adaptive filters for a given application
- b. Design multirate DSP Systems
- c. Implement adaptive signal processing algorithm
- d. Design active networks
- e. Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

#### **Text Books**:

- 1. "Digital Signal Processing, Principles, Algorithms and Applications", John G.Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.
- 2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.

#### **Reference books:**

- 4. "Modern Digital signal processing", Robert. O. Cristi, Cengage Publishers, India, 2003.
- 5. "Digital signal processing: A Practitioner's approach", E.C. Ifeachor, and B. W. Jarvis, , Second Edition, Pearson Education, India, 2002, Reprint.
- 6. "Wavelet Transforms, Introduction to Theory and applications", Raghuveer. M. Rao, Ajit S.Bopardikar, Pearson Education, Asia, 2000.

7.

## ERROR CONTROL CODING

As per choice based credit system(CBCS)scheme Semester – II			
Subject Code	17LDE22	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes etc and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Implement different Block code encoders and decoders.
- Analyze and implement convolutional encoders and decoders.
- Analyze and apply soft and hard Viterbi algorithm for decoding of convolutional codes.

Modules		Revised Bloom's Taxonomy(RBT) Level
Module-1 : Information theory:		
Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1) Introduction to algebra: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2m) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF (2m) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2)	10Hrs	L1, L2, L3
Module – 2 : Linear block codes:		
Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes(SPC), Repetition codes, Self dual codes, Hamming codes, Reed Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2)	10Hrs	L1, L2, L3
Module – 3: Cyclic codes:		
Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2).	10 Hrs	L1, L2, L3
Module – 4 : BCH Codes:		
BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic, Implementation of error	10 Hrs	L1, L2, L3

correction. (Chap. 6 of Text 2) 28 Reed -Solomon codes. (Chap. 7 of Text 2) Majority Logic decodable codes: One -step majority logic decoding, One-step majority logic decodable codes, Two-step majority logic, decoding, Multiple-step majority logic. (Chap. 8 of Text 2).		
Module – 5 : Convolution codes:		
Convolutional Encoding, Convolutional Encoder Representation, Formulation of the Convolutional Decoding Problem, Properties of Convolutional Codes: Distance property of convolutional codes, Systematic and Nonsystematic Convolutional Codes, Performance Bounds for Convolutional Codes, Coding Gain. Other Convolutional Decoding Algorithms: Sequential Decoding, Feedback Decoding.(Chap. 7 of Text 3)	10 Hrs	L1, L2, L3

- Analyse a discrete memoryless channel, given the source and transition probabilities.
- Apply the concept of modern linear algebra for the error control coding technique.
- Construct and Implement efficient LBC, Cyclic codes etc encoder and decoders.
- Apply decoding algorithms for efficient decoding of Block codes and Convolutional codes.

#### **Text Book:**

- Simon Haykin, "Digital Communication systems", First edition, Wiley India Private. Ltd, 2014. ISBN 978-81-265-4231-4
- 2. Shu Lin and Daniel J. Costello. Jr, "Error control coding", Pearson, Prentice Hall, 2nd edition, 2004.
- 3. Bernard Sklar, "Digital Communications Fundamentals and Applications", 2nd Edition Pearson Education (Asia) Ptv. Ltd, 2001.

- 1. Blahut. R. E, "Theory and practice of error control codes", Addison Wesley, 1984.
- 2. Salvatore Gravano, "Introduction to Error control coding", Oxford university press, 2007.

## WIRELESS COMMUNICATION

As per choice based credit system(CBCS)scheme Semester – II			
Subject Code	17LDN23	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- Characterize small-scale fading in terms of Doppler spectrum, coherence time, power delay profile, and coherence bandwidth.
- Apply mathematical models of radio wave propagation.
- Analyze the error probabilities for common modulation schemes.
- Describe different types of diversity and how they improve performance for mobile radio channels. Analyze the AWGN channel capacity.

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : The Wireless channel:			
Physical modeling for wireless channels, Input/output model of wireless channels, Time and frequency response, Statistical models. <b>10Hrs</b> (Text 1)		L1, L2, L3	
Module-2:Point-to-Point Communication, Detection diversity and c	hannel uncer	tainty:	
Detection in Rayleigh fading channels, Time diversity, Antenna diversity, Frequency diversity, Impact of the channel uncertainty. (Text 1)	10 Hrs	L1, L2, L3	
Module – 3: Diversity:			
Introduction Micro-diversity, Micro-diversity and Simulcast combination of signals, Error probability in fading channels with diversity reception, Transmit diversity. (Chap. 13 of Text2)	10 Hrs	L1, L2, L3	
Module – 4 : Capacity of wireless channel:			
AWGN channel capacity, Resources of AWGN channel, Linear time invariant Gaussian channel, Capacity of fading channels. (Text 1)	10 Hrs	L1, L2, L3	
Module – 5 : MIMO Systems:			
Introduction, Space diversity and system based on space diversity, Smart antenna systems and MIMO, MIMO based system architecture; MIMO exploits multipath, Space time processing, Antenna considerations for MIMO. MIMO channel modeling, MIMO channel measurements, MIMO channel capacity, CDD, Space time coding, advantages and applications of MIMO, MIMO application in 3G.(Chap. 15 of Text 3)	10 Hrs	L1, L2, L3	

- 1. Acquire knowledge of characteristics of mobile/wireless communication channels
- 2. Apply statistical models of multipath fading
- 3. Understand the multiple radio access techniques 30
- 4. Understand the need of coding, diversity, interleaving and link techniques for mo bile/wireless communications network
- 5. Design receiver and transmitter diversity techniques
- 6. Identify and describe modern techniques for high-rate wireless communications, using MIMO transmission.

#### **Text Books:**

- 1. David Tse, P. Vishwanath, "Fundamentals of Wireless Communication", Cambridge University press, 2006.
- 2. Andreas F.Molisch "Wireless Communications" 2nd Edition John Wiley & Sons.
- 3. Upena Dalal, "Wireless communication", Oxford, 2009.

#### **Reference Book:**

1. Ke-Lin Du, ad M.N.S. Swamy, "Wireless communication systems-From RF subsystems to 4G enabling Technologies", Cambridge

## **RF AND MICROWAVE CIRCUIT DESIGN**

As per choice based credit system(CBCS)scheme Semester – II			
Subject Code	17LDN24	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credit:04

- Understand waves propagating in Networks.
- Use the Smith Chart for various applications.
- Understand the basic considerations in active networks
- Design active networks.
- Understand RF/MW Frequency Mixer and Phase Shifter Design.

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Wave propagation in networks:			
Introduction, Reasons for Using RF/Microwaves, Applications, RF Waves, RF and Microwave circuit design, Introduction to Components Basics, Analysis of Simple Circuit in Phasor Domain, RF Impedance Matching, Transmission Media, High Frequency Parameters, Formulation of S-parameters, Properties of S-Parameters, Transmission Matrix, Generalized S-parameters.	10Hrs	L1, L2, L3	
Module – 2 : Smith chart and its Applications:			
Introduction, Smith Chart, Derivation of Smith Chart, Smith Chart Circular and Radial Scales, Application of Smith chart.	luction, Smith Chart, Derivation of Smith Chart, Smith Chart <b>10 Hours</b> lar and Radial Scales, Application of Smith chart.		
Module – 3: Basic consideration in active networks:			
Stability Considerations, Gain Considerations and Noise10 HourConsiderations.10 Hour		L1, L2, L3	
Module – 4 : RF/Microwave Amplifiers:			
Small Signal Design: Introduction, Types of amplifier, Design of different types of amplifiers RF/Microwave Frequency Conversion: Mixers: Introduction, Mixer Types, Conversion Losses for SSB Mixers, SSB versus DSB mixers, One diode mixers, Two diode Mixers	10 Hours	L1, L2, L3	
Module – 5 : RF/Microwave Control Circuit Design:			
Introduction, PN Junction Devices, Phase shifters, Digital phase shifters, Semiconductor phase shifters, PIN diode attenuators. RF and	10 Hours	L1, L2, L3	

Microwave IC design: MICs, MIC materials, Types of MICs, Hybrid	
verses Monolithic ICs, Chip mathematics	

- 1. Discuss and analyse waves propagation in Networks 32
- 2. Apply the Smith Chart for finding various parameters in transmission lines
- 3. Analyse the basic considerations in active networks
- 4. Describe and design active networks
- 5. Design RF/MW Frequency Mixers and phase shifters

#### **Text Book:**

1. Matthew M. Radmanesh, "RF and Microwave Electronics Illustrated", Pearson Education edition, 2004.

#### **Reference Book**:

1. Reinhold Ludwig, and Pavel Bretchko, "RF circuit design theory and applications", Pearson Education edition, 2004.

## WIRELESS & MOBILE NETWORKS

As per choice based credit system(CBCS)scheme Semester – I			
Subject Code	17LDN251	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit : 04

- a. Concepts and Protocols provides an explanation on the wireless network concepts, architectures, protocols, and applications.
- b. It covers the wireless networks such as wireless body area network (WBAN), wireless local area networks (WLANs),
- c. wireless metropolitan area networks (WMANs), wireless wide area network (WWAN), wireless sensor networks, wireless vehicle networks, and research challenges in wireless networks.
- d. Addresses the design issues and explores various emerging protocols for wireless networks
- e. Develop an awareness towards the network control and traffic management

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Review of fundamentals of wireless communication and	Networks:	
Wirelesscommunication channel specifications, Wireless communication systems, Wireless networks, Switching technology, Communication problems, Wireless network issues and standards.	10Hrs	L1, L2, L3, L4
Module - 2 : Wireless body area networks & Wireless personal area	a networks	
Properties, Network architectures, Components, Technologies, Design issues, Protocols and applications. Architectures, Components, Requirements, Technologies and protocols, Bluetooth and Zigbee	10 Hours	L1, L2, L3, L4
Module – 3: Wireless LANs		
Network components, design requirements, Architectures, IEEE- 802.11x, WLAN protocols, 802.11p and applications.	10 Hours	L2, L3, L4
Module – 4 : WMANs, IEEE-802.16		
Architectures, Components, WiMax mobility support, Protocols. Broadband networks and applications, WWANs, cellular networks, Satellite Network, Applications	10 Hours	L1, L2, L3, L4

Module – 5 : Wireless ad-hoc networks		
Mobile ad-hoc networks, Sensor network, Mesh networks, VANETs, Research issues in Wireless networks	10 Hours	L1, L2

- 1. Develop an understanding on the basic and advanced principles of Wireless Communications and Mobile Networks.
- 2. The unit addresses the issues of wireless communications and mobile networks in physical, link and network layers. The wireless channels will be explained with existing mitigation techniques.
- 3. Multi-user communication systems will also be studied with an emphasis on the broadcast nature of wireless communications.
- 4. Mobile networks modelling, design and optimisation will be covered, as well as existing and future mobile networks standard

- 1. S. S. Manvi, and M. S. Kakkasageri, "Wireless and Mobile network concepts and Protocols", Wiley, 1st edition, 2010.
- 2. P. Kaveh, Krishnamurthy, "Principles of Wireless network: A unified approach", PHI, 2006.
- 3. Iti Saha Mitra, "Wireless communication and network: 3G and Beyond", McGraw Hill, 2009.
- 4. Ivan Stojmenovic, "Handbook of Wireless networks and Mobile Computing", Wiley, 2009.
- 5. P. Nicopolitidis, M. S. Obaidat, et al, "Wireless Networks", Wiley, 2009.

### <u>MEMS</u>

As per choice based credit system(CBCS)scheme			
	Semester -	11	
Subject Code	17LDE252	CIE	50
Number of Lecture	02	SEE	50
Hours/Week	03	SEL	50
Total Number of	49 Even hours		211
Lecture Hours	40	Exam nours	51178

#### Credit:04

- a. Mathematically analyze and conceptualize basics of optical networking and its associated nonlinear artifacts and effects.
- b. Develop awareness regarding optical devices and their working strategies
- c. Develop awareness of WDM principles, and that of power penalty issues existent in optical Networks
- d. Get insight into the design of various types of Lasers and understand the techniques of coherent transmission.
- e. Develop an awareness towards the backbone architectures of optical networking with the present trends in access networks
- f. Design second generation optical networks using various existent & devices like OADM, OLT and OXC and to mathematically model the problems in the design of WDM networks

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Overview of MEMS & Microsystems:			
MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Microsystems design and manufacture, Applications of Microsystems in automotive industry, health care industry, aerospace industry, industrial products, consumer products and telecommunications.		L1, L2, L3	
Module – 2 : Scaling Laws in Miniaturization:			
Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces, electricity, scaling in fluid mechanics & heat transfer. <b>Transduction Principles in MEMS &amp; Microsystems:</b> Introduction,	10Hrs	L1, L2, L3	

Micro sensors — thermal, radiation, mechanical, magnetic and bio — sensors. Micro actuation. MEMS with micro actuators				
Module – 3: Microsystems Fabrication Process:				
Introduction, Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching and materials used for MEMS, Some MEMS fabrication processes: surface micro- machining, bulk micromachining, LIGA process, LASER micro machining, MUMPS, FAB-less fabrication	10 Hrs	L1, L2, L3,		
Module – 4 : Micro System Design and Modelin g:				
Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: ANSYS / Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, Design considerations of Optical MEMS (MOEMS), Design and Modeling: case studies - i) Cantilever beam ii) Micro switches iii) MEMS based SMART antenna in mobile applications for maximum reception of signal in changing communication conditions and iv) MEMS based micro mirror array for control and switching in optical communications.	10 Hrs	L1, L2, L3		
Module – 5 : Micro system packaging:				
Over view of mechanical packaging of micro electronics micro system packaging, Interfaces in micro system packaging, Packaging technologies	10 Hrs	L1, L2, L3		

- h. Recognize and select various optical networking components according to the prescribed design specifications Learn
- i. the aspects of data transmission, loss hindrances and other artifacts
- j. affecting the network operation
- k. the issues involved in setting up and maintenance of access part of optical
- 1. network with the latest trends in the data communication
- m. Design a WDM network and study the component and network management aspects

- 1. Tai Ran Hsu, "MEMS and Micro Systems : Design and Manufacture", Tata McGraw Hill, 2002
- 2. Boca Raton, "MEMS and NEMS: Systems, Devices and Structures", CRC Press, 2002
- 3. J. W. Gardner and V. K. Vardan, "Micro Sensors MEMS and SMART Devices", John Wiley, 2002
- 4. 4. N. Maluf "Introduction to Micro Mechanical Systems Engineering, Artech House", Norwood, MA, 2000.

### WIRELESS SENSOR NETWORKS

As per choice based credit system(CBCS)scheme				
Semester – I				
Subject Code	17LDN253 CIE 50			
Number of Lecture	03	SFF	50	
Hours/Week	05	SEE	50	
Total Number of	48 Even hours 2Une		10	211mg
Lecture Hours	40	Exam nours	SHIS	

#### Credit:04

- Explain sensor networks for various application setups.
- Demonstrate the design space and conduct trade-off analysis between performance and resources.
- Assess coverage and conduct node deployment planning.
- Devise appropriate data dissemination protocols and model links cost.
- Determine suitable medium access protocols and radio hardware.
- Illustrate sensor networks using commercial components.
- Discuss quality of service, fault-tolerance, security and other dependability requirements while coping with resource constraints.

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction:			
Overview and Applications of Wireless Sensor Networks Introduction, Basic overview of the Technology, Applications of Wireless Sensor Networks: Introduction, Background, Range of Applications, Examples of Category 2 WSN Applications, Examples of Category 1 WSN Applications, Another Taxonomy of WSN Technology. (Chapter 1: 1.1, 1.2, Chapter2: 2.1-2.6)	10Hrs	L1, L2, L3	
Module – 2 : Basic Wireless Sensor Technology and Systems:			
Introduction, Sensor Node Technology, Sensor Taxonomy, WN Operating Environment, WN Trends, Wireless Transmission Technology and Systems: Introduction, Radio Technology Primer, Available Wireless Technologies (Chapter 3: 3.1-3.5, Chapter 4: 4.1- 4.3)	10 Hours	L1, L2, L3	
Module – 3: MAC and Routing Protocols for Wireless Sensor Networks:			
Introduction, Background, Fundamentals of MAC Protocols, MAC	10 Hours	L1,L2, L3	

Protocols for WSNs, Sensor-MAC case Study, IEEE 802.15.4 LR-		
WPANs Standard Case Study. Routing Protocols for Wireless Sensor		
Networks: Introduction, Background, Data Dissemination and		
Gathering, Routing Challenges and Design Issues in WSNs, Routing		
Strategies in WSNs. (Chapter 5: 5.1-5.6, Chapter 6: 6.1-6.5)		
Module – 4 : Transport Control and Middleware for Wireless Sense	or Networks:	
Traditional Transport, Control Protocols, Transport Protocol Design		
Issues, Examples of Existing Transport Control Protocols,		
Performance of Transport Control Protocols. Middleware for	10 Hours	111713
Wireless Sensor Networks: Introduction, WSN Middleware		11, 12, 13
Principles, Middleware Architecture,		
Existing Middleware. (Chapter 7: 7.1-7.4, Chap. 8: 8.1-8.4)		
Module – 5 : Network Management and Operating System for Wire	eless Sensor 2	Networks:
Introduction, Network Management Requirements, Traditional		
Network Management Models, Network Management Design Issues.		
Operating Systems for Wireless Sensor Networks: Introduction,	10 Hours	L1, L2, L3
Operating System Design Issues, Examples of Operating		
Systems. (Chapter 9: 9.1-9.5, Chapter 10: 10.1-10.3).		

Course outcomes: The students shall able to:

- 1. Explain existing applications of wireless sensor actuator networks
- 2. Apply in the context of wireless sensor networks and explain elements of distributed computing and network protocol design
- 3. Contrast Various hardware, software platforms that exist for sensor networks
- 4. Summarize various network level protocols for MAC, routing, time synchronization, aggregation, consensus and distributed tracking.

#### **Text Book:**

2. KAZEM SOHRABY, DANIEL MINOLI, TAIEB ZNATI, "Wireless Sensor Networks: Technology, Protocols and Applications:, WILEY, Second Edition (Indian), 2014.

- 1. Ian F. Akyildiz, Mehmet Can Vuran "Wireless Sensor Networks", Wiley 2010
- 2. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.

## **CRYPTOGRAPHY AND NETWORK SECURITY**

As per choice based credit system(CBCS)scheme			
Semester – II			
Subject Code	17LDN254	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- Understand the basics of symmetric key and public key cryptography.
- Understand some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

Modules		Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction :			
<b>Foundations:</b> Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6) <b>SYMMETRIC CIPHERS:</b> Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4)	10Hrs	L1, L2, L3	
Module – 2 : Introduction to modular arithmetic:			
Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5) Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4)	10 Hours	L1, L2, L3	
Module – 3: Pseudo-Random-Sequence Generators and Stream Ciphers:			
Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	10 Hours	L1, L2, L3	

Module – 4 : One-Way Hash Functions:			
Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)		L1, L2, L3	
Module – 5 : E-mail Security:			
Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2). <b>IP Security:</b> IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP),Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4). <b>Web</b> <b>Security:</b> Web Security Considerations, SSL(Text 1: Chapter 15: Section 15.1, 15.2).	10 Hours	L1, L2, L3	

- 1. Use basic cryptographic algorithms to encrypt the data.
- 2. Generate some pseudorandom numbers required for cryptographic applications.
- 3. Provide authentication and protection for encrypted data

#### **Text Books:**

- 1. William Stallings, —Cryptography and Network Security Principles and Practicell, Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
- 2. Bruce Schneier, —Applied Cryptography Protocols, Algorithms, and Source code in C, Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

- 1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
- 2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

## **VLSI DESIGN FOR SIGNAL PROCESSING**

As per choice based credit system(CBCS)scheme Semester – II			
Subject Code	17LDN255	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
- Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Introduction to DSP Systems:		
Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.10HrsIteration Bounds: Data flow graph Representations, loop bound and Iteration bound.10Hrs		L1, L2, L3
Module – 2 : Iteration Bounds:		
Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs. <b>Pipelining and Parallel Processing:</b> pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.	10 Hours	L1, L2, L3
Module – 3: Retiming:	-	
Definition and Properties, Solving Systems of Inequalities, Retiming Techniques, <b>Unfolding</b> : An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. <b>Systolic Architecture Design:</b> systolic array design Methodology,FIR systolic array.	10 Hours	L1, L2, L3
Module – 4 : Systolic Architecture Design:		
Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays.	10 Hours	L1, L2, L3

<b>Fast convolution</b> : Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.		
Module – 5 : Pipelined and Parallel Recursive and Adaptive Filter:		
Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter	10 Hours	L1, L2, L3

- 1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
- 2. Use pipelining and parallel processing in design of high-speed /low-power applications
- 3. Apply unfolding in the design of parallel architecture
- 4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
- 5. Develop an algorithm or architecture or circuit design for DSP applications

#### **Text Books:**

1. Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

- 1 Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.
- 2 S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing ", Prentice Hall, 1985.
- 3 Jose E. France, Yannis Tsividis, " Design of Analog Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
- 4 Lars Wanhammar, —DSP Integrated Circuits<sup>II</sup>, Academic Press Series in Engineering, 1st Edition.

## ADVANCED DSP LAB

As per choice based credit system(CBCS)scheme				
	Semester – I			
Laboratory Code	17LDNL26	CEE	50	
Number of Leadure		SEE	50	
Hours/Week	06	Exam hours	3Hrs	

#### Credits :02

Course objectives: This laboratory course enables students to get practical experience

• Matlab implementation of LTI systems and multirate systems

• Realization of some systems using DSP 6713 processor

#### PART-A: Experiments to be done using MATLAB

1. Computation of Linear convolution, Circular convolution, Linear convolution using circular convolution L1,L2, L3

- 2. Computation of DFT, IDFT, Circular convolution in frequency domain
- 3. Comparison of DFT and DCT (in terms of energy compactness)

Generate the sequence x[n]=n-64 for n=0, ...127.

(a) Let  $X[k] = DFT\{x[n]\}$ . For various values of l, set to zero "high

frequency coefficients"  $X[64-1] = \dots X[64] = \dots X[64+L] = 0$  and take the inverse DFT. Plot the results.

(b) Let XDCT[k]=DCT(X[n]). For the same values of L, set to zero "high frequency coefficient" XDCT [127-L]= ....XDCT[127]. Take the inverse DCT for each case and compare the reconstruction with the previous case.

- 4. Determination of power spectrum density of a given sequence
- 5. Generation of DTMF Signals
- 6. Implementation of Decimation Process and Implementation of Interpolation Process
- 7. Time-Frequency Analysis with the Continuous Wavelet Transform
- 8. Signal Reconstruction from Continuous Wavelet Transform Coefficients
- 9. Denoising Signals and Images
- 10.Haar Wavelet Image Compression

#### PART-B: Experiments to be done using the DSP processor

1. Write an ALP to obtain the response of a system using linear convolution whose input and impulse response are specified. L1,L2, L3

- 2. Write an ALP to obtain the impulse response of the given system, given the difference equation.
- 3. Computation of FFT when N is not a power of 2.
- 4. Synthesis of Dual Tone Multi Frequency using 6713 processor

**Course outcomes:** On the completion of this laboratory course, the students will be able to:

- 1. Realize the following using Matlab
- · Response of LTI systems.
- $\cdot$  DFT and DCT
- $\cdot$  Decimation
- $\cdot$  Wavelet Transforms
- 2. Implement the following using 6713 processor
- · Response of LTI systems and convolution.
- $\cdot$  FFT realization and DTMF generation.

## WIRELESS BROADBAND COMMUNICATIONS

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code17LDN41CIE50			
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credits : 04

- Explain the system architecture of LTE and E-UTRAN as per the standards
- Understand the Multiple Access process incorporated in the radio physical layer.
- Associate MAC of LTE radio interface protocols to set up, reconfigure and release
- the Radio Bearer and for transferring to the EPS bearer.
- Explain the mobility principles and procedures in the idle and active state.
- Analyse the main factors affecting LTE performance including mobile speed and transmission bandwidth.

Modules		Revised Bloom's Taxonomy(RBT) Level
Module-1 : LTE		
LTE Standardization Phases, Evolution Beyond Release 8, LTE-		
Advanced for IMT-Advanced, LTE Specifications and 3GPP		
Structure.		
System Architecture Based on 3GPP SAE:		
Basic System Architecture Configuration with only E-UTRAN	10Hrs	L2, L3
Access Network, System Architecture with E-UTRAN and Legacy		
3GPP Access Networks, System Architecture with E-UTRAN and		
Non-3GPP Access Networks, Architecture Configuration, IMS		
Architecture, PCC and QoS.		
Module – 2 : Introduction to OFDMA, SC-FDMA and MIMO in LT	E:	
LTE Multiple Access Background, OFDMA Basics, SC-FDMA		
Basics MIMO Basics.		
Physical Layer:	10	
Transport Channels and their Mapping to the Physical Channels,	Hours	L2, L3
Modulation, Uplink User Data Transmission, Downlink User Data		
Transmission, Uplink Physical Layer Signaling Transmission,		
PRACH Structure, Downlink Physical Layer Signaling Transmission.		

Module – 3: Physical Layer		
Physical Layer Procedures, UE Capability Classes and Supported		
Features		
Physical Layer Measurements, Physical Layer Parameter Configuration.	10	
LTE Radio Protocols:	Hours	L1, L2, L3
Protocol Architecture, The Medium Access Control The Radio Link		
Control		
Layer, Packet Data Convergence Protocol.		
Module – 4 : Radio Resource Control (RRC:		
Radio Resource Control (RRC): X2 Interface Protocols		
Understanding the RRC ASN.1 Protocol Definition, Early UE		
Handling in LTE.		1213
Mobility:	110015	L2, L3
Mobility Management in Idle State, Intra-LTE Handovers 190, Inter-		
system Handovers Differences in E-UTRAN and UTRAN Mobility.		
Module – 5 : Radio Resource Management:		
Overview of RRM Algorithms, Admission Control and QoS		
Parameters, Downlink Dynamic Scheduling and Link Adaptation,		
Uplink Dynamic Scheduling and Link Adaptation, Interference	Hours	L1, L2, L3
Management and Power Settings, Discontinuous Transmission and		
Reception (DTX/DRX), RRC Connection Maintenance.		

- 1. Understand the system architecture and the function standard specified components of the system of LTE 4G.
- 2. Analyze the role of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from a number of users.
- 3. Demonstrate the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios.
- 4. Test and Evaluate the Performance of resource management and packet data processing and transport algorithms.

#### **Text Book:**

1. 'LTE for UMTS Evolution to LTE-Advanced' HarriHolma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003.

- 1. 'Fundamentals of LTE', by Arunabha Ghosh, Jun Zhang, Jeffrey G. Andrews), Rias Muhamed, 1st Edition, Sept 2010, Prentice Hall Communications Engineering and Emerging Technologies Series from Ted Rappaport, ISBN13: 9780137033119, ISBN10: 0137033117.
- 'EVOLVED PACKET SYSTEM (EPS) ; THE LTE AND SAE EVOLUTION OF 3G UMTS' by Pierre Lescuyer and Thierry Lucidarme, 2008, John Wiley & Sons, Ltd. Print ISBN:978-0-470-05976-0.
- **3.** 'LTE The UMTS Long Term Evolution ; From Theory to Practice' by Stefania Sesia, IssamToufik, and Matthew Baker, 2009 John Wiley & Sons Ltd, ISBN 978-0-470-69716-0.

## **CMOS RF CIRCUIT DESIGN**

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code	17LVE421	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours48Exam hours3Hrs			

#### Credit:04

- Learn basic concepts in RF and microwave design emphasising the effects of nonlinearity and noise.
- Able to appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Able to deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level			
Module-1 : Introduction to RF Design and Wireless Technology:					
Basic concepts in RF design (I): General considerations, Effects					
of	10Hrs	L1, L2, L3			
Nonlinearity, Noise, Sensitivity and dynamic range,					
Module – 2 :					
<b>Basic concepts in RF design (II)</b> : Passive impedance transformation, scattering parameters, analysis of nonlinear	10Hrs	L1, L2, L3			
dynamic systems					
Module – 3: Communication Concepts:	Module – 3: Communication Concepts:				
General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards	10 Hrs	L1, L2, L3			
Module – 4 : Transceiver Architecture (I):					
General considerations, Receiver architecture,	10 Hrs	L1, L2, L3			
Module – 5 : Transceiver Architecture (II):					
Transmitter architectures	10 Hrs	L1, L2, L3			

Low Noise Amplifiers: LNA topologies: common-source stage	
with inductive load, common-source stage with resistive feedback.	
Mixers: General considerations, passive down conversion mixers.	

- Analyse the effect of nonlinearity and noise in RF and microwave design.
- Exemplify the approaches taken in actual RF products.
- Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.
- Explain various receivers and transmitter topologies with their merits and drawbacks.
- Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

#### **Text Book**:

1. B. Razavi, "RF Microelectronics", PHI, second edition.

- **1.** R. Jacob Baker, H.W. Li, D.E. Boyce "CMOS Circuit Design, layout and Simulation", PHI 1998.
- 2. Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.
- 3. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996.

### **ADVANCES IN IMAGE PROCESSING**

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code17LDN422CIE50			
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credit:04

- To gain fundamental knowledge in understanding the representation of the digital image and its properties
- To equip students with some pre-processing techniques required to enhance the image for further analysis purpose.
- To enable students to select the region of interest in the image using segmentation techniques.
- To enable students to represent the image based on its shape and edge information.
- To enable student to describe the objects present in the image based on its properties and structures.

Modules		Revised Bloom's Taxonomy(RBT) Level
Module-1 : The image, its representations and properties:		
Image representations a few concepts, Image digitization, Digital image properties, Color images.	10Hrs	L1
Module-2: Image Pre-processing		
Pixel brightness transformations, geometric transformations, local	10 Hrs	L1. L2
pre-processing		,
Module – 3: Segmentation:		
Thresholding; Edge-based segmentation – Edge image		
thresholding, Edge relaxation, Border tracing, Hough transforms;	10 11	
Region – based segmentation – Region merging, Region splitting,	10 Hrs	L1, L2, L3
Splitting and merging, Watershed segmentation, Region growing		
post-processing.		

Module – 4 : Shape representation and description		
Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms Of boundaries, Boundary description using segment sequences, Bspline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	10 Hrs	L1, L2, L3
Module – 5 : Mathematical Morphology:		
Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.	10 Hrs	L1, L2, L3

- 1. Understand the representation of the digital image and its properties Apply pre-processing techniques required to enhance the image for its further analysis.
- 2. Use segmentation techniques to select the region of interest in the image for analysis
- 3. Represent the image based on its shape and edge information.
- 4. Describe the objects present in the image based on its properties and structure.
- 5. Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects..

### Text Book:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0.

- 1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
- 2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata Mc Graw Hill, 2011

## COMMUNICATION SYSTEM DESIGN Using DSP ALGORITHMS

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code17LDN423CIE50			
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

### Credit:04

- Introduce communication systems, including algorithms that are particularly suited to DSP implementation.
- Introduced Software and hardware tools, as well as FIR and IIR digital filters and the FFT.
- Discusses modulators and demodulators for classical analog modulation methods such as amplitude modulation (AM), doublesideband suppressed-carrier amplitude modulation (DSBSC-AM), single sideband modulation (SSB), and frequency modulation (FM).
- Explore digital communication methods leading to the implementation

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level	
Module-1 : Introduction			
<b>Introduction to the course</b> : Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.	10Hrs	L1, L2	
Module – 2 : Analog modulation scheme			
Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal. Envelope detection and square law detection. Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation. DSBSC: Theory generation of DSBSC, Demodulation, and	10 Hours	L1, L2	

demodulation using coherent detection and Costas loop.			
Implementation of DSBSC using DSP hardware.			
SSB: Theory, SSB modulators, Coherent demodulator, Frequency			
translation, Implementation using DSP hardware. (Text 1, 2)			
Module – 3: Frequency modulation:			
Theory, Single tone FM, Narrow band FM,			
FM bandwidth, FM demodulation, Discrimination and PLL			
methods, Implementation using DSP hardware.			
Digital Modulation scheme: PRBS, and data scramblers:			
Generation of PRBS, Self -synchronizing data scramblers,	10 Hours	L1, L2, L3	
Implementation of PRBS and data scramblers. RS-232C protocol			
and BER tester: The protocol, error rate for binary signaling on the			
Gaussian noise channels, Three bit error rate tester and			
implementation.			
Module – 4 : PAM and QAM:			
PAM theory, baseband pulse shaping and ISI, Implementation of			
transmit filter and interpolation filter bank. Simulation and			
theoretical exercises for PAM, Hardware exercises for PAM.			
<b>QAM fundamentals:</b> Basic QAM transmitter, 2 constellation	10 Hours	111212	
examples, QAM structures using passband shaping filters, Ideal		121, 122, 123	
QAM demodulation, QAM experiment. QAM receivers-Clock			
recovery and other frontend sub-systems. Equalizers and carrier			
recovery systems.			
Module – 5 : RF/Microwave Control Circuit Design:			
Experiment for QAM receiver frontend. Adaptive equalizer, Phase			
splitting, Fractionally spaced equalizer. Decision directed carrier			
tracking, Blind equalization, Complex cross coupled equalizer and			
carrier tracking experiment.	10 Hours	111213	
Echo cancellation for full duplex modems: Multicarrier	10 110015	11, 12, 13	
modulation, ADSL architecture, Components of simplified ADSL			
transmitter, A simplified ADSL receiver, Implementing simple			
ADSL Transmitter and Receiver.			

Upon successful completion of this course the students will be able to:

- a. Understand and implement DSP algorithms on TI DSP processors
- b. Implement and make use of FIR and IIR digital filtering. And FFT methods
- c. Analyse and implement modulators and demodulators for AM,DSBSCAM, SSB and FM
- **d.** Understand and design digital communication methods leading to the implementation of a line communication system.

#### **Text Book:**

1. Tretter, Steven A., "Communication System Design Using DSP Algorithms With Laboratory Experiments for the TMS320C6713<sup>™</sup> DSK", Springer USA, 2008.

- 1. Robert. O. Cristi, "Modern Digital signal processing", Cengage Publishers, India, 2003.
- 2. S. K. Mitra, "Digital signal processing: A computer based approach", 3rd edition, TMH, India, 2007.
- 3. E.C. Ifeachor, and B. W. Jarvis, "Digital signal processing: A Practitioner's approach", Second Edition, Pearson Education, India, 2002,
- 4. Proakis, and Manolakis, "Digital signal processing", 3rd edition, Prentice Hall, 1996.

## **RECONFIGURABLE COMPUTING**

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code	17LDE424	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

Course objectives: The aim of this course is to enable the students to

- Acquire fundamental knowledge and understanding of principles and practice in reconfigurable architecture.
- Understand the FPGA design principles, and logic synthesis.
- Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
- f. Focus on different domains of applications on reconfigurable computing.

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Introduction		
History, Reconfigurable Vs Processor based system,		
RC Architecture. Reconfigurable Logic Devices: Field		
Programmable Gate Array, Coarse Grained Reconfigurable		
Arrays.	10Hrs	L1, L2
Reconfigurable Computing System: Parallel Processing on		
Reconfigurable Computers, A survey of Reconfigurable		
Computing System. Text(1)		
Module – 2 : Wireless body area networks & Wireless personal area networks		
<b>Languages and Compilation:</b> Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging	10 Hours	L1, L2

Reconfigurable Computing Applications.			
Text(1)			
Module – 3: Implementation			
Implementation: Integration, FPGA Design flow, Logic			
Synthesis.	10 Hours	111212	
High Level Synthesis for Reconfigurable Devices: Modelling,	10 110015	L1, L2, L3	
Temporal Partitioning Algorithms. (Text 2).			
Module – 4 : Partial Reconfiguration Design:			
Partial Reconfiguration Design, Bitstream Manipulation with			
JBits, The modular Design flow, The Early Access Design	10 11		
Flow, Creating Partially Reconfigurable Designs, Partial	10 Hours	L1, L2	
Reconfiguration using Hansel-C Designs, Platform			
Design. (Text 2)			
Module – 5 : Signal Processing Applications			
Reconfigurable computing for DSP, DSP application building			
blocks, Examples: Beamforming, Software Radio, Image and			
video processing, Local Neighbourhood functions, Convolution.	10 Hours	111213	
(Text 1)	10 110015	L1, L2, L3	
System on a Programmable Chip: Introduction to SoPC,			
Adaptive Multiprocessing on Chip. (Text 2)			

- a. Simulate and synthesize the reconfigurable computing architectures.
- b. Use the reconfigurable architectures for the design of a digital system.
- c. Design of digital systems for a variety of applications on signal processing and system on chip configurations. Reference books

#### **Text Books**:

- 1. M. Gokhale and P. Graham, —Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays, Springer, 2005.
- 2. C. Bobda, —Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications, Springer, 2007.

- 1. D. Pellerin and S. Thibault, —Practical FPGA Programming in Cl, Prentice-Hall, 2005.
- 2. W. Wolf, -FPGA Based System Design, Prentice-Hall, 2004.
- 3. R. Cofer and B. Harding, —Rapid System Prototyping with FPGAs: Accelerating the Design Processl, Newnes, 2005.

## ADVANCED MICROCONTROLLERS

As per choice based credit system(CBCS)scheme Semester – IV			
Subject Code	17LDE425	CIE	50
Number of Lecture Hours/Week	03	SEE	50
Total Number of Lecture Hours	48	Exam hours	3Hrs

#### Credit:04

- a. Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc.
- b. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation.
- c. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.
- d. Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

Modules	Teaching Hours	Revised Bloom's Taxonomy(RBT) Level
Module-1 : Overview of Microcontrollers :		
<b>Motivation for advanced microcontrollers</b> – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.	10Hrs	L1, L2, L3
Module – 2 : MSP430 – 16-bit Microcontroller family.		
CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus – architecture. The assembly language and "C" programming for MSP-430 microcontrollers. On-chip	10Hrs	L1, L2, L3

peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts.		
Module – 3:		
<b>ARM -32 bit Microcontroller family.</b> Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.	10 Hrs	L1, L2, L3,
Module – 4 : Digital Input-Output and Serial Communication:		
Parallel Ports, Lighting LEDs, Flashing LEDs, Read Input from a Switch, Toggle the LED state by pressing the push button, LCD interfacing. Asynchronous Serial Communication, Asynchronous Communication with USCI_A, Communications, Peripherals in MSP430, Serial Peripheral Interface. (Text: Selected topics from Ch4 & Ch7 and Ch7- 7.1, Ch10 – 10.1, 10.2, and 10.12)	10 Hrs	L1, L2, L3
Module – 5 : Applications :		
Wireless Sensor Networking with MSP430 and Low-Power RF circuits: Pulse Width Modulation(PWM) in Power Supplies	10 Hrs	L1, L2, L3

- a. Understand the architectural features and instruction set of 16 bit microcontroller MSP430.
- b. Develop programs using the various instructions of MSP430 for different applications.
- c. Understand the functions of the various peripherals which are interfaced with MSP430 microcontroller
- d. Describe the power saving modes in MSP430. Explain the low power applications using MSP430 microcontroller.

- 1. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3, , Newnes, (Elsevier), 2008.
- 2. John Davies, "MSP430 Microcontorller Basics", Newnes (Elsevier Science), 2008.
- 3. MSP430 Teaching CD-ROM, Texas Instruments, 2008.
- 4. Sample Programs for MSP430 downloadable from msp430.com
- 5. David Patterson and John L. Henessay, "**Computer Organization and Design**", (ARM Edition), Morgan Kauffman.
- Chris Nagy, Embedded Systems Design using TI MSP430 Series, Newnes Publications, Elsevier, 2003. 2. User Guide from Texas Instruments.



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