FACULTY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Title of the Event	Five-Day Faculty Development Program (FDP) "End-to-End IC Design Flow Using Cadence Tools"
Date of Activity held	16/06/2026 to 20/06/2026
Time of Activity	10:00 AM - 5:00 PM
Type of Activity (Cultural/ Co-curricular/Curricular)	Curricular Activity
Resource Person	• Mr. Rakesh B R • Mr. Nandish Cadence India
Professional details of Resource Person	• Field Application Engineer at Trellisign Technologies Pvt Ltd • Principal Application Engineer at Cadence Design Systems
Program/Course/ Class	Faculty Development Program
Number of faculties attended	79
Activity Incharge	Dr. Anuradha Savadi Dr Rekha S Dr Mahesh R K Prof. Shruti V H, Prof. Shweta Biradar
Introduction	The Department of Electronics and Communication Engineering organized a Five-Day Faculty Development Programme (FDP) on "End-to-End IC Design Flow Using Cadence Tools" with the objective of enhancing the knowledge and practical skills of faculty members, research scholars, and postgraduate students in modern VLSI design methodologies. The programme focused on the complete custom IC design flow beginning from circuit specifications to GDSII generation using the Cadence design environment and PCB design using OrCAD tool. Industry experts delivered technical sessions complemented by extensive laboratory demonstrations.
Objective of the activity	• To provide faculty members with a comprehensive understanding of Analog and Digital VLSI Design. • To familiarize participants with modern VLSI design methodologies and industry practices. • To introduce EDA tools used in front-end and back-end VLSI design. • To introduce OrCAD tool used for circuit design and PCB layout design. • To enhance teaching and research capabilities in semiconductor and VLSI domains. • To bridge the gap between academic curriculum and industry requirements.

Description of Activity	The Faculty Development Program (FDP) aims to provide hands-on experience and theoretical understanding of VLSI design methodologies, focusing on Full-Custom and Semi-Custom design flows using Cadence EDA tools**.** This two-day program is structured to enhance teaching and research capabilities of faculty members in the area of integrated circuit (IC) design. The sessions include expert lectures, tool demonstrations, and lab sessions involving schematic design, layout creation, DRC/LVS checks, and digital implementation techniques.
Software Used	• Cadence Virtuoso • Cadence Spectre • ADE Explorer • ADE Assembler • Pegasus/Assura (DRC & LVS) • Quantus QRC (Parasitic Extraction) • Voltus-Fi (EM/IR Drop) • OrCAD
	

Date	Session Time	Resource Person	Topic
16/06/26	10: 00 AM to 11: 00 AM	Mr. Rakesh B R Field Application Engineer Trellisign Technologies Pvt. Ltd. Bangalore	Inauguration
16/06/26	11: 30 AM to 01: 00 PM		Introduction to Full Custom IC Design Flow
16/06/26	2: 00 PM to 4: 00 PM		Layout Design, Post Layout Simulation, Timing, Power Analysis and Generation of GDSII
17/06/26	10: 30 AM to 01: 00 PM		Introduction to Semi-Custom IC Design Flow
17/06/26	2: 00 PM to 4: 30 PM		Physical Implementation using Innovus
18/06/26	10: 30 AM to 01: 00 PM		Introduction to Full Custom IC Design Flow for FinFET Technology
18/06/26	2: 00 PM to 4: 30 PM		Layout Design, Physical Verification which includes DRC & LVS, Parasitic Extraction using Quantus and Post Layout Simulation
19/06/26	10: 30 AM to 01: 00 PM		Overview of OrCAD tool,
19/06/26	2: 00 PM to 4: 30 PM		Introductive to OrCAD PCB Editor, Setting up board outline, grids, and design constraints and Component placement and routing
20/06/26	10: 30 AM to 01: 00 PM	Mr. Nandish Math, Principal Application Engineer, Cadence Design System, Bangalore	Emerging Trends and Industry Perspective
20/06/26	2: 00 PM to 3: 30 PM		Research Opportunities in VLSI
20/06/26	3: 30 PM to 4: 30 PM		Valedictory Session and Certificate Distribution

Registration Link :
https://forms.gle/7DdWBYGcGG65qRz26

Note: Certificates will be issued to participants on attending all the sessions

Registration Fee:
Faculty/Research Scholar: 1000/-

A/C Holder Name: Chancellor FO conference Sharnbasva University Klb
A/C No.: 209321010000025
IFSC: UBIN0920932
Bank Name: Union Bank of India, Vidya Nagar Branch Klb.

Co-Convenors
Dr. Shashidar Sonnad
Chairperson Dept.ECE (Co-Ed)
Dr. Nagveni K
Chairperson Dept.ECE (Ex-Women)

Co-Ordinators
Dr. Anuradha Savadi Assoc. Prof.
Dr. Rekha S Assoc. Prof.
Dr. Mahesh R K Asst. Prof.
Prof. Shruti V H Asst. Prof.
Prof. Shweta Biradar Asst. Prof.

With the Benign Blessing of
His Holiness Vidya Bhandari
Lingaikya Poojya Dr. Sharnbaswappa Appa
8th Mahadasoha Peethadhipati, Shambaveshwar Samsthan, Kalaburagi
Founder Chancellor, Sharnbasva University, Kalaburagi
Founder Trustee, Poojya Dr. Sharnbaswappa Appa Family Trust

Chief-Patrons
Poojya Matoshree Dr. Dakshayini S. Appa
Hon'ble Chancellor, Sharnbasva University, Kalaburagi
President, Shambaveshwar Vidya Vardhaka Sangha, Kalaburagi
Trustee, Poojya Dr. Sharnbaswappa Appa Family Trust

Poojya Shri. Doddappa S. Appa
9th Mahadasoha Peethadhipati, Shambaveshwar Samsthan, Kalaburagi
Trustee, Poojya Dr. Sharnbaswappa Appa Family Trust

Patrons
Shri. Basavaraj S Deshmukh
Secretary Shambaveshwar Vidya Vardhak Sangha
Member, BOG, Sharnbasva University, Kalaburagi

Dr. Anilkumar G. Bidve
Vice Chancellor, Sharnbasva University, Kalaburagi

Convenors
Dr. Lakshmi Patil
Registrar, Sharnbasva University, Kalaburagi
Chairman, IETE, Kalaburagi Center

Dr. Shivakumar Jawaligi
Dean, Sharnbasva University, Kalaburagi

Resource persons
Mr. Rakesh B R
Field Application Engineer Trellisign Technologies Pvt., Ltd., Bangalore

Mr. Nandish Math
Principal Application Engineer, Cadence Design System, Bangalore

Advisory Committee

Dr. V D Mytri Director, SUK
Dr. S H Honnalli Registrar (Eval),SUK
Dr. Kiran Maka Finance officer, SUK
Dr. Vinita Patil Principal, Lingaraj Appa Engineering College, Gornalli, Bidar
EC Member, IETE, Kalaburagi Center
Dr. Sharanbasappa Sali Principal, Veerappa Nisty Engineering College, Shorapur
Dr. Sujata Mallapur Dean of research, SUK
Secretary, IETE, Kalaburagi Centre
Dr. Shilpa Shrigiri Professor Dept. Of ECE
Dr. Basanti Ghanti Professor, Dept. Of ECE
Dr. Ravindrakumar Nagarale Prof. Dept. Of ECE
Dr. Savita Patil Prof. Dept. Of ECE
Dr. Revati Godi Prof. Dept. Of ECE
Prof. Shivganga Patil Assoc. Prof. Dept. Of ECE
Dr. Sujata K Assoc. Prof. Dept. Of ECE

About University

Sharnbasva University, located in Kalaburagi, Karnataka, India, is a multidisciplinary private university established in 2017 with the objective of providing quality higher education, promoting research, and contributing to societal development. The university is recognized by the University Grants Commission (UGC), the statutory body responsible for maintaining standards of higher education in India.

The establishment of Sharnbasva University marked a significant milestone in the educational development of the Kalyana-Karnataka region, which historically required expanded access to higher education and advanced research facilities. The university aims to create a vibrant academic ecosystem where students can acquire knowledge, develop professional competencies, and cultivate ethical and social values. With its strong commitment to academic excellence, innovation, and community engagement, Sharnbasva University strives to prepare students to meet global challenges while contributing positively to society.

About Department

Department of Electronics and Communication Engineering offer courses that cover fundamental concepts in electronics, such as Semiconductor Devices, analog and digital circuits, Electronic Communication Systems, electromagnetic theory, VLSI, Embedded programming and signal processing etc. These courses form the basis of understanding for students pursuing degrees in Electronics and Communication Engineering.

Department of Electronics & Communication Engineering provides a strong foundation in technical and theoretical aspects. ECE department provides abundant opportunities for students to wok on self - designed mini projects, develop communication skills, explore internship opportunities in the industry and take part in national and international conferences. The ECE department is committed to promote research, industrial interaction. the department is associated with professional bodies like IEEE, ISTE and IETE for faculty and students to enhance their research activities. The department has an excellent placement track record with attractive salary packages.

About FDP

The Department of Electronics and Communication Engineering (ECE) organizes Faculty Development Programmes (FDPs) on End- to - End IC design flow using Cadence Tool to enhance the knowledge and technical skills of faculty members, researchers and postgraduate students. These programmes focus on emerging trends in semiconductor technology, integrated circuit (IC) design, System-on-Chip (SoC) development, FPGA implementation, verification methodologies and Electronic Design Automation(EDA) tools.

The FDP typically includes expert lectures from industry, hands-on training using industry-standard tools such as Cadence and discussions on current research challenges in VLSI design. Participants gain exposure to digital design flow, physical design, verification techniques and advanced semiconductor technologies.

Objectives:

- To provide faculty members with a comprehensive understanding of Analog and Digital VLSI Design.
- To familiarize participants with modern VLSI design methodologies and industry practices.
- To introduce EDA tools used in front-end and back-end VLSI design.
- To enhance teaching and research capabilities in semiconductor and VLSI domains.
- To bridge the gap between academic curriculum and industry requirements.

Sharnbasva University
Kalaburagi - 585 103

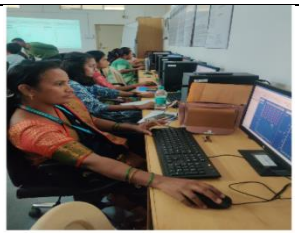
CERTIFICATE OF PARTICIPATION
PROUDLY PRESENTED TO

of

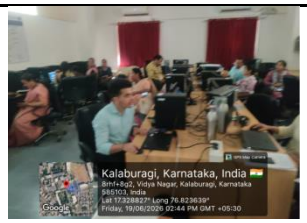
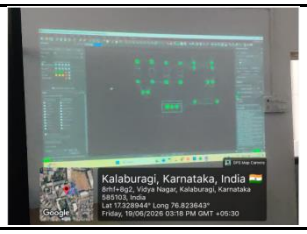
has successfully completed Five Days Faculty Development Programme on "End-to-End IC Design Flow Using Cadence Tools" Organized by Department of Elcectronics & Communication Engineering, Faculty of Engineering & Technology, in Association with Trellisign Technologies Pvt. Ltd. Bengaluru from 16/06/2026 to 20/06/2026.

DEAN REGISTRAR VICE CHANCELLOR

Day 1 **June 16, 2026**	**Inaugural function** **Session-1: (11 am - 1 pm)** • Introduction to Full Custom IC Design Flow • Cadence Solutions for Custom IC Design • MOSFET Characterization • Schematic Capture using Virtuoso Schematic Editor • Symbol Creation • Testbench Creation using Virtuoso Schematic Editor • Functional Simulation using Spectre **Session-2: (2 pm - 4 pm)** • Layout Design using Virtuoso • Layout Editor Physical Verification which includes DRC & LVS • Parasitic Extraction using Quantus • Post Layout Simulation • Timing Analysis • Power Analysis

	• Generation of GDSII **Note:** By considering, CS-Amplifier as an example will demonstrate the entire Full Custom IC Design Flow. **(4 pm - 5 pm)** **Discussions**         
Day 2 **June 17, 2026**	**Session-1: (10 am - 1 pm)** • Introduction to Semi-Custom IC Design Flow • Cadence Solutions for Semi-Custom IC Design • Functional Verification using Incisive • Coverage Analysis using IMC • RTL Synthesis using Genus Synthesis Solution • Logic equivalence Check using Conformal **Session-2: (2 pm - 4 pm)** • Physical Implementation using Innovus that includes Floor Planning, Power Planning, Placement, CTS, Routing • Timing Analysis • Power Analysis • Generation of GDSII **(4 pm - 5 pm)** **Discussions**   
Day 3 **June 18, 2026**	**Session-1: (10 am - 1 pm)** • Introduction to Full Custom IC Design Flow • Cadence Solutions for Custom IC Design

	• MOSFET Characterization • Schematic Capture using Virtuoso Schematic Editor • Symbol Creation • Testbench Creation using Virtuoso Schematic Editor • Delay and Power estimation • Functional Simulation using Spectre **Session-2: (2 pm - 4 pm)** • Layout Design using Virtuoso • Layout Editor Physical Verification which includes DRC & LVS • Parasitic Extraction using Quantus • Post Layout Simulation • Generation of GDSII **Note:** The session will be demonstrated by Using FinFET (18nm) and NAND Gate as an example. **Note:** By considering, Memory as an example will demonstrate the entire Semi-Custom IC Design Flow. **(4 pm - 5 pm)** **Discussions** 
Day 4 **June 19, 2026**	**Session 1: (10 am - 1 pm)** ● Overview of OrCAD tool. ● Library Creation ● Creating a new schematic project ● Adding and editing components from the library ● Introduction to PSpice simulation environment ● Running simulations and analyzing waveforms ● BOM Generation ● Transferring the schematic to PCB Editor (Netlist generation) **Session 2: (2 pm - 4 pm)** ● Introduction to OrCAD PCB Editor ● Setting up board outline, grids, and design constraints ● Component placement and routing ● Design rule checks (DRC) and error fixing ● Gerber File Generation **(4 pm - 5 pm)** **Discussions**

	  
Day 5 **June 20, 2026**	**Emerging Trends and Industry Perspective** **Session 1: (10 am - 1 pm)** • Research Opportunities in VLSI **Session 2: (2 pm - 4 pm)** • Valedictory Session and Certificate Distribution      
Course Outcome	Analyze and implement the complete custom IC design flow using Cadence tools, including schematic design, simulation, layout, physical verification, and post-layout validation for fabrication-ready integrated circuits.
Outcome of the Activity	The FDP successfully provided comprehensive knowledge of the " End-to-End Custom IC Design Flow" using Cadence tools. The combination of theoretical concepts and extensive practical sessions significantly enhanced participants' understanding of modern semiconductor design methodologies. The programme bridged the gap between academic learning and industrial practices, enabling faculty members to incorporate advanced VLSI design concepts into teaching and research.
Conclusion	The Five-Day FDP on "End-to-End IC Design Flow Using Cadence Tools" successfully achieved its objectives by providing participants with comprehensive exposure to the complete custom IC design process. The programme enhanced participants' technical competencies in schematic design, simulation, layout, physical verification, post-layout analysis, and tape-out methodology using industry-standard Cadence tools. The knowledge gained through this FDP will contribute significantly to quality teaching, research, and industry-oriented curriculum development in the field of VLSI and Semiconductor Engineering.

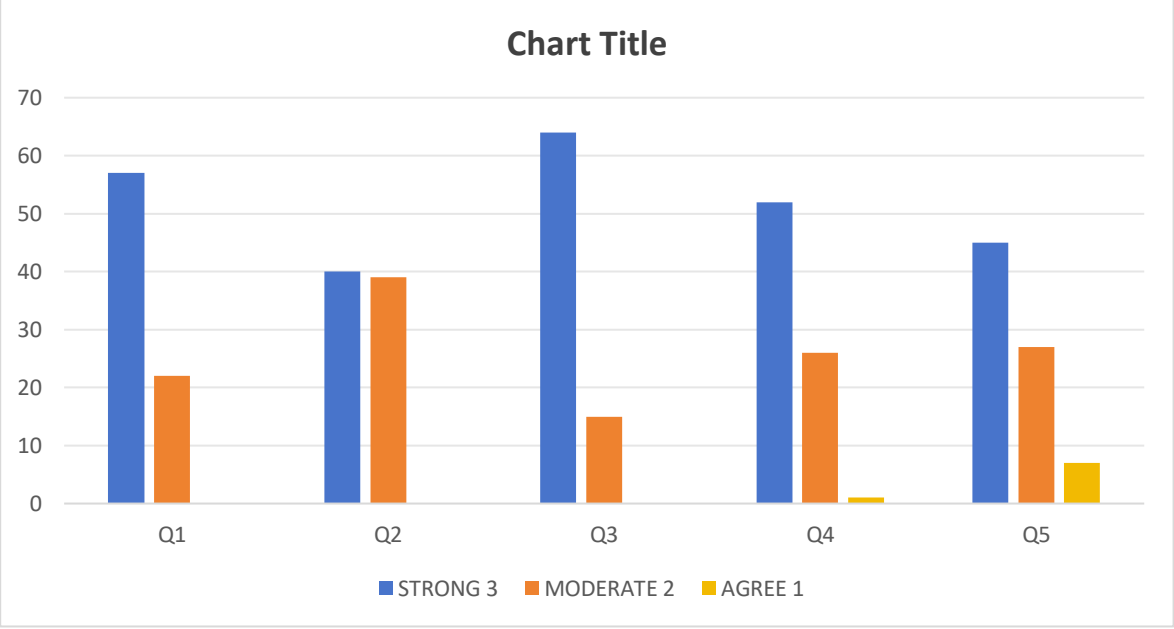
CO's, PO's and PSO's Correlation

CO's No.	CO Defined	Relevance to PO's and PSO'S
CO	Analyze and implement the complete custom IC design flow using Cadence tools, including schematic design, simulation, layout, physical verification, and post-layout validation for fabrication-ready integrated circuits.	PO1, PO2, PO3, PO4, PO5, PO9,PO10,PO11

Title of the Event: End-to-End IC Design Flow Using Cadence Tools.

Number of faculties attended: 79

Q. No	Strongly Agree (3)		Moderately Agree (2)		Agree(1)		Total Score	%Attainment = (Total score/Total no. Students attended)	Average percentage Attainment	Attainment levels	Mapped POs	Mapped PSOs
1.	57	171	22	44	0	0	215	2.72	87.66	STRONG = 3	1,2,3,4,5,9,10,11	
2.	40	120	39	78	0	0	198	2.50				
3.	64	192	15	30	0	0	222	2.81				
4.	52	156	26	52	1	1	209	2.64	87.66			
5.	45	135	27	54	7	7	196	2.48				
Average								2.63				



Impact Analysis: From the above table, Awareness Program on Five days Faculty Development Program on Strongly attained to level 3. Against mapped PO1, PO2, PO3, PO4, PO5, PO9,PO10,P11. Note: High=3, Moderate=2 and Low=1

Coordinator **Chairperson** **Dean**