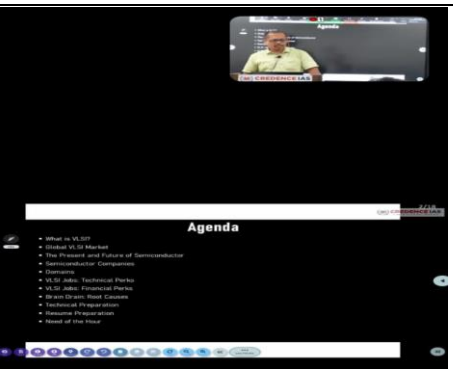
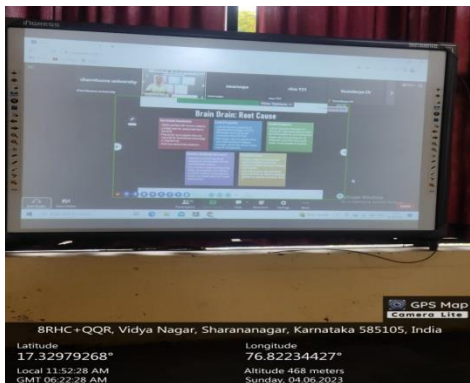


Faculty of Engineering and Technology (Exclusively for Women)

Department of Electronics & Communication Engineering

Title of the Event	Expert talk on "VLSI Career Insights and Opportunities"
Date of Activity held	4/06/2023
Time of Activity	11.00pm to 12.30pm.
Type of Activity (Cultural/ Co-curricular/Curricular)	Co curricular Activity
Resource Person	Mr. Ravi Siddanath
Professional details of Resource Person	Principal Engineer at Broadcom Inc.
Program/Course/ Class	B.Tech. ECE
Number of Staff attended	5
Activity Incharge	Prof. Shruti V H
Objective of the activity	To provide engineering students with insights into the current trends, technologies, and career opportunities in the field of Very-Large-Scale Integration (VLSI) and to bridge the gap between academic learning and industry expectations.
Description of Activity	The speaker highlighted the importance of VLSI in modern electronic systems, discussed the design and manufacturing flow, and elaborated on various roles available in the field such as front-end design, back-end design, verification, testing, and fabrication.
Course Outcome	Understand the scope and professional opportunities in the field of VLSI design and its relevance to current industry trends.
Outcome of the Activity	- Students will gain exposure to real-world VLSI applications and design processes. - They will understand the skillsets required to pursue a career in VLSI and semiconductor domains. - Students will be able to identify internship and job opportunities in the VLSI industry.
Activity Photographs	   

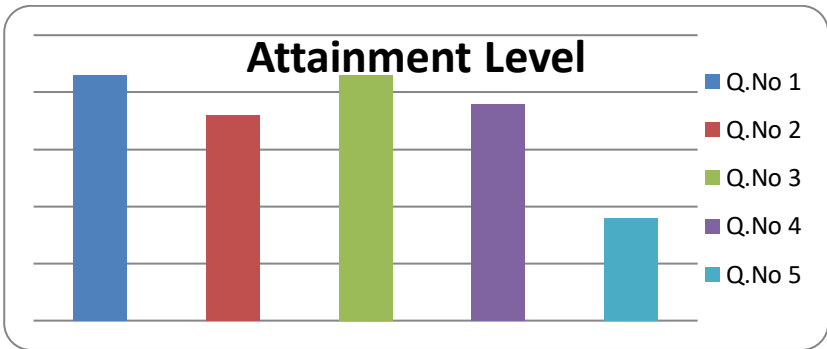
CO's, PO's and PSO's Correlation

CO's No.	CO Defined	Relevance to PO's and PSO'S
CO	Understand the scope and professional opportunities in the field of VLSI design and its relevance to current industry trends.	PO6, PO7, PO8, PO12 and PSO3

Title of the Event: Expert talk on “VLSI Career Insights and Opportunities”

Number of Students: 44

Q. No	Strongly Agree (3)		Moderately Agree (2)		Agree(1)		Total Score	%Attainment = (Total score/Total no. Students attended)	Average percentage Attainment	Attainment levels	Mapped POs	Mapped PSOs
1.	26	78	07	14	11	11	103	2.34	79.4	Medium = 2	6, 7, 8, 12	3
2.	27	81	08	16	09	09	106	2.40				
3.	28	84	07	14	09	09	107	2.43				
4.	27	81	07	14	10	10	105	2.38				
5.	26	78	08	16	10	10	104	2.36				
Average								2.38				



Impact Analysis: From the above table, Expert talk on “VLSI Career Insights and Opportunities” moderately attained to level 2. Against mapped PO6, PO7, PO8, PO12 and PSO3. Note: High=3, Moderate=2 and Low=1

Coordinator

Chairperson

Dean